European Low-Power Initiative for Electronic System Design

Designing CMOS Circuits for Low Power

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esprit

DIMES
Delft Institute of Microelectronics and Submicron Technology

DESIGNING CMOS CIRCUITS FOR LOW POWER

Based on selected partner contributions of the European Low Power Initiative for Electronic System Design of the European Community ESPRIT4 programme and other

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Foreword

This book is the fourth in a series on novel low power design architectures, methods and design practices. It results from of a large European project started in 1997, whose goal is to promote the further development and the faster and wider industrial use of advanced design methods for reducing the power consumption of electronic systems.

Low power design became crucial with the wide spread of portable information and communication terminals, where a small battery has to last for a long period. High performance electronics, in addition, suffers from a permanent increase of the dissipated power per square millimeter of silicon, due to the increasing clock-rates, which causes cooling and reliability problems or otherwise limits the performance.

The European Union's Information Technologies Programme 'Esprit' did therefore launch a 'Pilot action for Low Power Design', which eventually grew to 19 R&D projects and one coordination project, with an overall budget of 14 million EURO. It is meanwhile known as European Low Power Initiative for Electronic System Design (ESD-LPD) and will be completed in the year 2002. It involves to develop or demonstrate new design methods for power reduction, while the coordination project takes care that the methods, experiences and results are properly documented and publicised.

The initiative addresses low power design at various levels. This includes system and algorithmic level, instruction set processor level, custom processor level, RT-level, gate level, circuit level and layout level. It covers data dominated and control dominated as well as asynchronous architectures. 10 projects deal mainly with digital, 7 with analog and mixed-signal, and 2 with software related aspects. The principal application areas are communication, medical equipment and e-commerce devices.

The following list describes the objectives of the 20 projects. It is sorted by decreasing funding budget.

CRAFT CMOS Radio Frequency Circuit Design for Wireless Application

- Advanced CMOS RF circuit design including blocks such as LNA, down converter mixers & phase shifters, oscillator and frequency synthesiser, integrated filters delta sigma conversion, power amplifier
- Development of novel models for active and passive devices as well as fine-tuning and validation based on first silicon fabricates
- Analysis and specification of sophisticated architectures to meet in particular low power single chip implementation

PAPRICA Power and Part Count Reduction Innovative Communication Architecture

- Feasibility assessment of DQIF, through physical design and characterisation of the core blocks
- Low-power RF design techniques in standard CMOS digital process
- RF design tools and framework; PAPRICA Design Kit.
- Demonstration of a practical implementation of a specific application

MELOPAS Methodology for Low Power Asic design

- To develop a methodology to evaluate the power consumption of a complex ASIC early on in the design flow
- To develop a hardware/software co-simulation tool
- To quickly achieve a drastic reduction on the power consumption of electronic equipment

TARDIS Technical Coordination and Dissemination

- To organise the communication between design experiments and to exploit their potential synergy
- To guide the capturing of methods and experiences gained in the design experiments
- To organise and promote the wider dissemination and use of the gathered design know-how and experience

LUCS Low Power Ultrasound Chip Set.

- Design methodology on low power ADC, memory and circuit design
- Prototype demonstration of a handheld medical ultrasound scanner

ALPINS Analog Low Power Design for Communications Systems

- Low-voltage voice band smoothing filters and analog-to-digital and digital-to-analog converters for an analog front-end circuit of a DECT system
- High linear transconductor-capacitor (gm-C) filter for GSM Analog Interface Circuit operating at supply voltages as low as 2.5V
- Formal verification tools, which will be implemented in the industrial partners design environment. These tools support the complete design process from system level down to transistor level

SALOMON System-level analog-digital trade-off analysis for low power

- A general top-down design flow for mixed-signal telecom ASICs
- High-level models of analog and digital blocks and power estimators for these blocks
- A prototype implementation of the design flow with particular software tools to demonstrate the general design flow

DESCALE Design Experiment on a Smart Card Application for Low Energy

- The application of highly innovative handshake technology
- Aiming at some 3 to 5 times less power and some 10 times smaller peak currents compared to synchronously operated solutions

SUPREGE A low power SUPerREGEnerative transceiver for wireless data transmission at short distances

- Design trade-offs and optimisation of the micro power receiver / transmitter as a function of various parameters (power consumption, area, bandwidth, sensitivity, etc)
- Modulation / demodulation and interface with data transmission systems
- Realisation of the integrated micro power receiver / transmitter based on the super-regeneration principle

PREST Power REduction for System Technologies

- Survey of contemporary Low Power Design techniques and commercial power analysis software tools
- Investigation of architectural and algorithmic design techniques with a power consumption comparison
- Investigation of Asynchronous design techniques and Arithmetic styles
- Set-up and assessment of a low power design flow
- Fabrication and characterisation of a Viterbi demonstrator to assess the most promising power reduction techniques

DABLP Low Power Exploration for Mapping DAB Applications to Multi-Processors

- A DAB channel decoder architecture with reduced power consumption
- Refined and extended ATOMIUM methodology and supporting tools

COSAFE Low Power Hardware-Software Co-Design for Safety-Critical Applications

- The development of strategies for power efficient assignment of safety critical mechanisms to hardware or software
- The design and implementation of a low-power, safety-critical ASIP, which realises the control unit of a portable infusion, pump system

AMIED Asynchronous Low-Power Methodology and Implementation of an Encryption/Decryption System

- Implementation of the IDEA encryption/decryption method with drastically reduced power consumption
- Advanced low power design flow with emphasis on algorithm and architecture optimisations
- Industrial demonstration of the asynchronous design methodology based on commercial tools

LPGD A Low-Power Design Methodology/Flow and its Application to the Implementation of a DCS1800-GSM/DECT Modulator/Demodulator

- To complete the development of a top-down, low power design methodology/flow for DSP applications
- To demonstrate the methods at the example of an integrated GFSK/GMSK Modulator-Demodulator (MODEM) for DCS1800-GSM/DECT applications

SOFLOPO Low Power Software Development for Embedded Applications

- Develop techniques and guidelines for mapping a specific algorithm code onto appropriate instruction subsets
- Integrate these techniques into software for the power-conscious ARM-RISC and DSP code optimisation

I-MODE Low Power RF to Base band Interface for Multi-Mode Portable Phone

- To raise the level of integration in a DECT/DCS1800 transceiver, by implementing the necessary analog base band low-pass filters and data converters in CMOS technology using low power techniques

COOL-LOGOS Power Reduction through the Use of Local don't Care Conditions and Global Gate Resizing Techniques: An Experimental Evaluation.

- To apply the developed low power design techniques to the existing 24-bit DSP, which is already fabricated
- To assess the merit of the new techniques using experimental silicon through comparisons of the projected power reduction (in simulation) and actually measured reduction of new DSP; assessment of the commercial impact

LOVO Low Output VOltage DC/DC converters for low power applications

- Development of technical solutions for the power supplies of advanced low power systems, comprising the following topics
- New methods for synchronous rectification for very low output voltage power converters

PCBIT Low Power ISDN Interface for Portable PC's

- Design of a PC-Card board that implements the PCBIT interface
- Integrate levels 1 and 2 of the communication protocol in a single ASIC
- Incorporate power management techniques in the ASIC design:
  - system level: shutdown of idle modules in the circuit
  - gate level: precomputation, gated-clock FSMs

COLOPODS Design of a Cochlear Hearing Aid Low-Power DSP System

- Selection of a future oriented low-power technology enabling future power reduction through integration of analog modules
- Design of a speech processor IC yielding a power reduction of 90% compared to the 3.3 Volt implementation

The low power design projects have achieved the following results:

- Projects, who have designed a prototype chip, can demonstrate a power reduction of 10 to 30 percent.
- New low power design libraries have been developed.
- New proven low power RF architectures are now available.
- New smaller and lighter mobile equipment is developed.

Instead of running a number of Esprit projects at the same time independently of each other, during this pilot action the projects have collaborated strongly. This is achieved mostly by the novelty of this action, which is the presence and role of the coordinator: DIMES - the Delft Institute of Microelectronics and Submicron-technology, located in Delft, the Netherlands (http://www.dimes.tudelft.nl). The task of the coordinator is to co-ordinate, facilitate, and organize:

- The information exchange between projects.
- The systematic documentation of methods and experiences.
- The publication and the wider dissemination to the public.

The most important achievements, credited to the presence of the coordinator are:

- New personnel contacts have been made, and as a consequence the resulting synergy between partners resulted in better and faster developments.
- The organization of low power design workshops, special sessions at conferences, and a low power design web site, http://www.esdlpd.dimes.tudelft.nl. At this site all public reports of the projects can be found and all kind of information about the initiative itself.
- The used design methodology, design methods and/or design experience are disclosed, are well documented and available.

  Based on the work of the projects, in cooperation with the projects, the publication of a low power design book series is planned. Written by members of the projects this series of books on low power design will disseminate novel design methodologies and design experiences, which were obtained during the runtime of the European Low Power Initiative for Electronic System Design, to the general public.

In conclusion, the major contribution of this project cluster is that, except the already mentioned technical achievements, the introduction of novel knowledge on low power design methods into the mainstream development processes is accelerated.

We would like to thank all project partners from all the different companies and organizations who make the Low Power Initiative a success.

Rene van Leuken, Reinder Nouta, Alexander de Graaf, Delft, May 2002

Introduction

Modern electronic systems have reached a significant turning point in the last decade, from low performance products such as wristwatches and calculators to high performance products such as laptops and personal digital assistants. The introduction of these devices to the consumer market raised to the surface a characteristic that had been previously omitted. This was low power dissipation. Gradually, engineers invented novel techniques, which may be included in efficient design methodologies, for designing and implementing efficient circuits not only in terms of area and performance, as they were used to, but in the term of low power consumption.

The material in this book is based on the background and the innovative results of the different partners involved in the AMIED, LPGD, PREST, COSAFE, and LUCS projects of the European Low Power Initiative for Electronic System Design under the successful coordination of DIMES, Delft. The partners have been studying for many years low-power design field introducing novel concepts and efficient techniques. Due to close collaboration of academic and industrial research groups the presented material have been influenced by the plethora of disseminations e.g. public deliverables, technical meetings, workshops, during the projects execution.

The book consists of two parts: The first part includes the low power design techniques for power optimization and estimation, while the second one provides the results from the projects COSAFE and LUCS. Starting from the description of the power consumption sources, low power optimization and estimation techniques for logic design level, circuit/transistor design level, and layout design level are provided in eight chapters (i.e. Chapters 2-9). The next two chapters describe the novel low power techniques, which were used during the implementation of the safety-critical Application Specific Instruction Processor designed in COSAFE project, and the implementation of the low power 16-channel ultrasound beamformer application specific integrated circuit (ASIC) designed for LUCS project.

A top-down approach with respect to the design level is adopted in the presentation of the low power design techniques . However,it was not possible to present in detail manner all the low power optimization and estimation techniques from the logic level to the layout level. Only the most important research contributions presented in a tutorial manner, are included. The book can also be used as a textbook for undergraduate and graduate students, VLSI design engineers,and professionals, who have had a basic knowledge of VLSI digital design.

The authors of the chapters of this book together with the editors would like to use this opportunity to thank the many people, i.e. colleagues and Ph.D. students, whose dedication and industry during the projects execution lead to the introduction of novel scientific results and realization of innovative integrated systems.

The authors of Chapter 3 and 9 would like to thank Dr. S. Theoharis for his contribution in the software development of logic optimization and estimation tools, which were necessary for making power measurements.

The authors of Chapter 6 wish to acknowledge the discussions with Dr. Karagianni, who significantly influenced the particular chapter. Also the authors appreciate the financial support from the "C. Caratheodory's" fund for the University of Patras.

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All authors of this book together with the editors would like to thank DIMES, Delft, for their continuous support during the running of the low power projects for the dissemination of the scientific results. This book is one of the activities of this dissemination task.

The authors of Chapter 4 would like to thank the people, who contributed to PREST, whose public deliverable reports used as an inspiration source for chapter's preparation.

Last but not least, D. Soudris would like to thank his parents for being a constant source of moral support and for firmly imbibing into him from a very young age that *perseverantia omnia vincit* - it is this perseverance that kept him going. This book is dedicated to them.

Dimitrios Soudris, Christian Piguet, Costas Goutis, May 2002

Chapter 5

CIRCUIT TECHNIQUES FOR REDUCING POWER CONSUMPTION IN ADDERS AND MULTIPLIERS

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Abstract An important issue in the design of VLSI Circuits is the choice of the basic circuit approach and topology for implementing various logic and arithmetic functions such as adders and multipliers. In this chapter, several static and dynamic CMOS circuit design styles are evaluated in terms of area, propagation delay and power dissipation. The different design styles are compared by performing detailed transistor-level simulations on a benchmark circuit (ripple carry adder) using HSPICE, and analyzing the results in a statistical way. After the comparison between the different design styles, a number of well known types of adders (ripple carry, carry skip, carry lookahead, carry select etc.) are compared in terms of propagation delay, number of gates and logic transition's average number. Furthermore, power measurements and comparisons for a number of well-known multipliers are provided. Based on the results of the provided analysis some of the tradeoffs that are possible during the design phase in order to improve the circuit power-delay product are identified.

Keywords: circuit design techniques, circuit macroblocks, adders, circuit styles

5.1 Introduction

Much of the research efforts of the past years in the area of digital electronics has been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters [1]. The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. Hence, in recent VLSI systems the power-delay product becomes the most essential metric of performance.

The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. In this chapter, the proper circuit style and methodology is considered. Since, most digital circuitry is composed of simple and/or complex gates, we study the best way to implement adders in order to achieve low power dissipation and high speed. Several circuit design techniques are compared in order to find their efficiency in terms of speed and power dissipation. A review of the existing CMOS circuit design styles is given, describing their advantages and their limitations. Furthermore, a four-bit ripple carry adder for use as a benchmark circuit was designed in a full-custom manner by using the different design styles, and detailed transistor-level simulations using HSPICE [2] were performed. Also, various designs and implementations of four multipliers are analysed in the terms of delay and power consumption. Two ways of power measurements are used.

Conventional static CMOS has been a technique of choice in most processor design. Alternatively, static pass transistor circuits have also been suggested for low-power applications [3]. Dynamic circuits, when clocked carefully, can also be used in low-power, high speed systems [4]. However, several other design techniques need to be applied and evaluated along with these circuit styles in order to improve the speed and reduce the power dissipation of VLSI systems. In this chapter we study eight different CMOS logic styles:

- Conventional Static CMOS - *CSL*,
- Complementary Pass-transistor - *CPL* [5],
- Double Pass-transistor - *DPL* [6],
- Static and Dynamic Differential Cascode Voltage Switch - *DCVSL* [7,8],
- Static Differential Split-level - *SDSL* [9],
- Dual-Rail Domino - *DRDL* [10,11], and
- Enable/disabled CMOS Differential - *ECDL* [12].

The rest of the chapter is structured as follows. In the next section a brief introduction of the power dissipation and the delay in CMOS circuits is given. In section 3, the CMOS adder logic styles and their characteristics are described in details. The different adder logic styles are compared in terms of speed, power dissipation and silicon area, in section 4. Also, the power-delay product of the designs is considered, due to the importance of this metric in modern VLSI applications. Comparison results among different realizations of a 16-bit adder in terms of area, delay, and power are presented in Section 6. The next section provides results for four implementations of multipliers. Finally, the main points are summarized in Section 7 of conclusions.

5.2 Power and Delay in CMOS Circuits

Since the objective is to investigate the tradeoffs that are possible at the circuit level in order to reduce power dissipation while maintaining the overall system throughput, we must first study the parameters that affect the power dissipation and the speed of a circuit. It is well known that one of the major advantage of CMOS circuits over single polarity MOS circuits, is that the static power dissipation is very small and limited to leakage. However, in some cases such as bias circuitry and pseudo-nMOS logic, static power is dissipated. Considering that in CMOS circuits the leakage current between the diffusion regions and the substrate is negligible, the two major sources of power dissipation are the switching and the short-circuit power dissipation [1],

$$P = p_f \, C_L \, V_{dd}^2 \, f \;\; + \;\; I_{sc} \, V_{dd}, \tag{5.1}$$

where p_f is the node transition activity factor, C_L is the load capacitance, V_{dd} is the supply voltage,f is the switching frequency. I_{sc} is the current which arises when a direct path from power supply to ground is caused, for a short period of time during low to high or high to low node transitions [13]. The switching component of power arises when energy is drawn from the power supply to charge parasitic capacitors. It is the dominant power component in a well designed circuit and it can be lowered by reducing one or more of p_f, C_L, V_{dd} and f, while retaining the required speed and functionality.

Even though the exact analysis of circuit delay is quite complex, a simple first-order derivation can be used [14,15] in order to show its dependency of the circuit parameters

$$T_d \;\; \propto \;\; \frac{C_L \, V_{dd}}{K \;\; (V_{dd} - V_{th})^{\alpha}}, \tag{5.2}$$

where K depends on the transistors aspect ratio (W/L) and other device parameters, V_{TH} is the transistor threshold voltage, and α is the velocity saturation index which varies between 1 and 2 (α is equal to 1.4 for the 1.5μm process

technology which is used in the experiments of the next section). Since a quadratic improvement in power dissipation may be obtained by lowering the supply voltage (equation (5.1)), many researchers have investigated the effects of lowering the supply voltage in VLSI circuits. Unfortunately, reducing the supply voltage reduces power, but the delay increases (equation (5.2)) with the effect being more drastic at voltages close to the threshold voltage [16]. Equations (5.1) and (5.2) indicate that by reducing the node parasitic capacitance in a CMOS circuit, the power dissipation is reduced and the circuit speed is increased.

5.3 CMOS Circuit Design Styles

In the following, the circuit design styles are described using the full adder circuit, which is the most commonly used cell in arithmetic units. Also, their characteristics in terms of power dissipation and delay are investigated.

5.3.1 Conventional Static CMOS Logic - CSL

Conventional Static CMOS logic is used in most chip designs in the recent VLSI applications. The schematic diagram of a conventional static CMOS full adder cell is illustrated in Figure 5.1. The signals noted with "-" are the complementary signals. The pMOSFET network of each stage is the dual network of the nMOSFET one. In order to obtain a reasonable conducting current to drive capacitive loads the width of the transistors must be increased. This results in increased input capacitance and therefore high power dissipation and propagation delay.

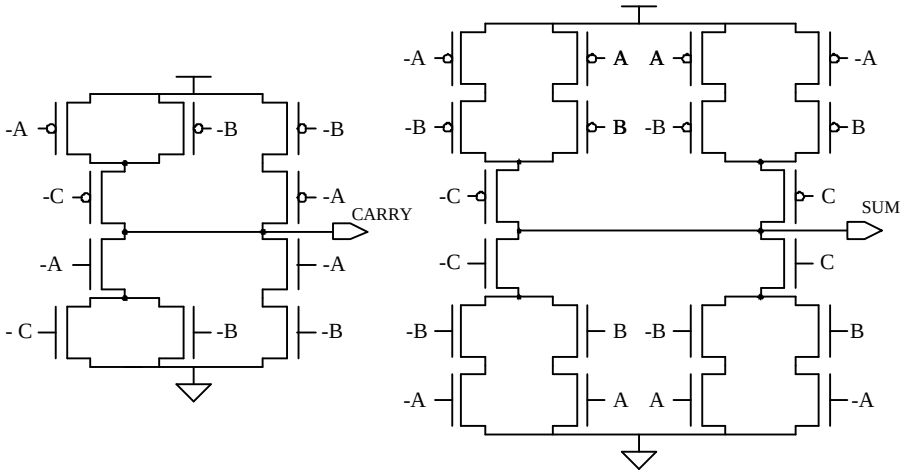

Figure 5.1. Conventional static CMOS full adder

5.3.2 Complementary Pass-Transistor Logic - CPL

The main concept behind CPL [5] is the use of only an nMOSFET network for the implementation of logic functions. This results in low input capacitance and high speed operation. The schematic diagram of the CPL full adder circuit is shown in Figure 5.2. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level. The switching power dissipated from charging or discharging the pass transistor outputs is given by

$$P_D = V_{dd}\, V_{swing}\, C_{node}\, f, \tag{5.3}$$

where $V_{swing} = V_{dd} - V_{thn}$. In the case of conventional static CMOS circuits the voltage swing at the output nodes is equal to the supply voltage, resulting in higher power dissipation. To minimize the static current due to the incomplete turn-off of the pMOSFET in the output inverters, a weak pMOSFET feedback device can also be added in the CPL circuits of Figure 5.2, in order to pull the pass-transistor outputs to full supply voltage level. However, this will increase the output node capacitance, leading to higher switching power dissipation and higher propagation delay.

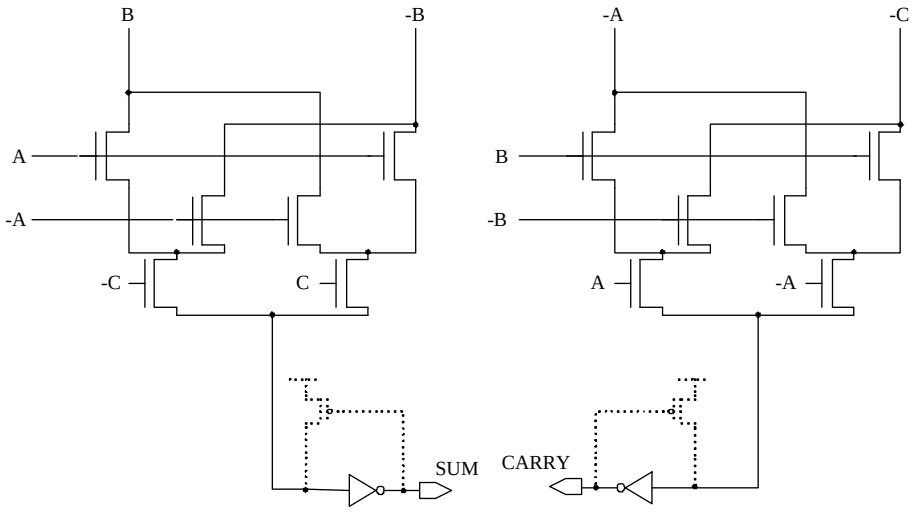

Figure 5.2. Complementary pass-transistor full adder

5.3.3 Double Pass-Transistor Logic - DPL

DPL [6] is a modified version of CPL. The circuit diagram of the DPL full adder is given in Figure 5.3. In DPL circuits full-swing operation is achieved by simply adding pMOSFET transistors in parallel with the nMOSFET transistors. Hence, the problems of noise margin and speed degradation at reduced supply voltages which are caused in CPL circuits due to the reduced high voltage level, are avoided. However, the addition of pMOSFETs results in increased input capacitances.

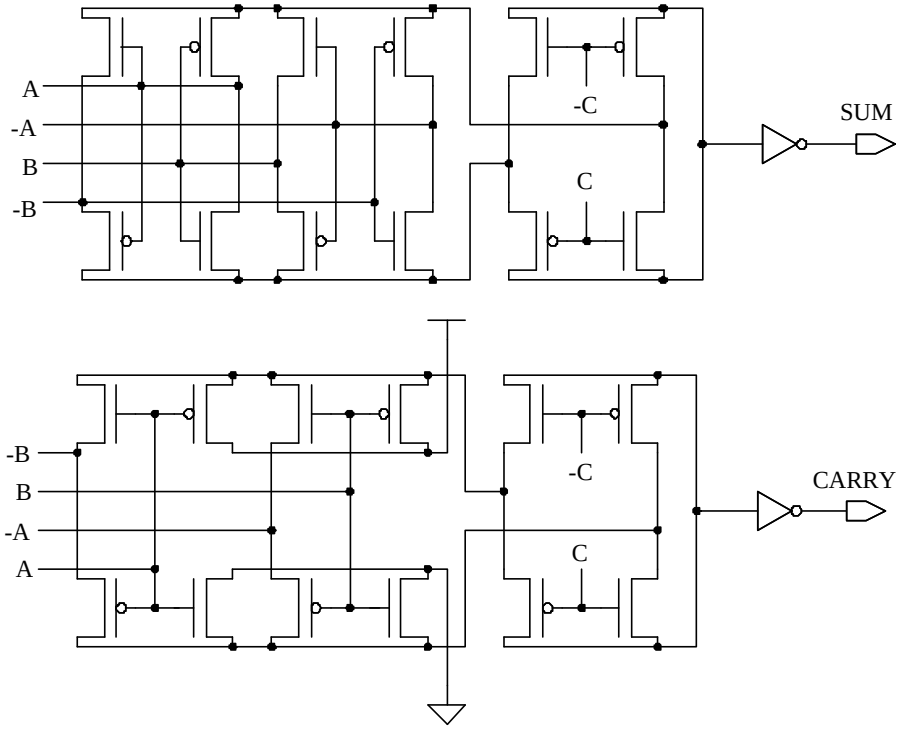

Figure 5.3. Double pass-transistor full adder

5.3.4 Static Differential Cascode Voltage Switch Logic - SDCVSL

Static DCVSL [7], is a differential style of logic requiring both true and complementary signals to be routed to gates. Figure 5.4 shows the circuit diagram of the static DCVSL full adder. Two complementary nMOSFET switching trees are constructed to a pair of cross-coupled pMOSFET transistors. Depending on

the differential inputs one of the outputs is pulled down by the corresponding nMOSFET network. The differential output is then latched by the cross-coupled pMOSFET transistors. Since the inputs drive only the nMOSFET transistors of the switching trees, the input capacitance is typically two or three times smaller than that of the conventional static CMOS logic.

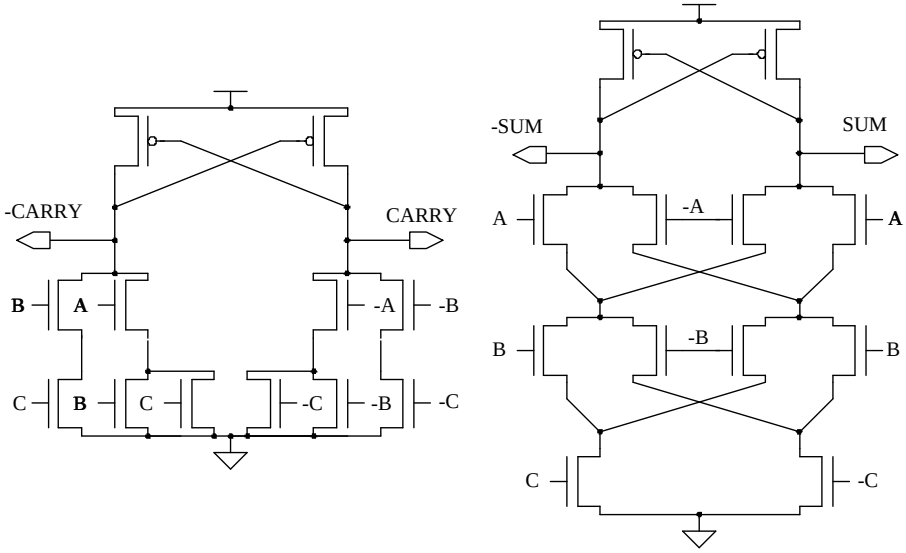

Figure 5.4. Static differential cascode voltage switch full adder

5.3.5 Static Differential Split-level Logic - SDSL

A variation of the differential logic described above is the Static DSL [9]. The SDSL full adder circuit diagram is illustrated in Figure 5.5. Two nMOSFET transistors with their gates connected to a reference voltage ($V_{ref} = (V_{dd}/2) + V_{thn}$, V_{thn}: nMOSFET threshold voltage) are added to reduce the logic swing at the output nodes. The output nodes are clamped at the half of the supply voltage level. Thus, the circuit operation becomes faster than standard DCVSL circuits. However, due to the incomplete turn-off of the cross-coupled pMOSFET transistors, SDSL circuits dissipate high static power dissipation. Also, the addition of two extra nMOSFET transistors per gate results in area overhead.

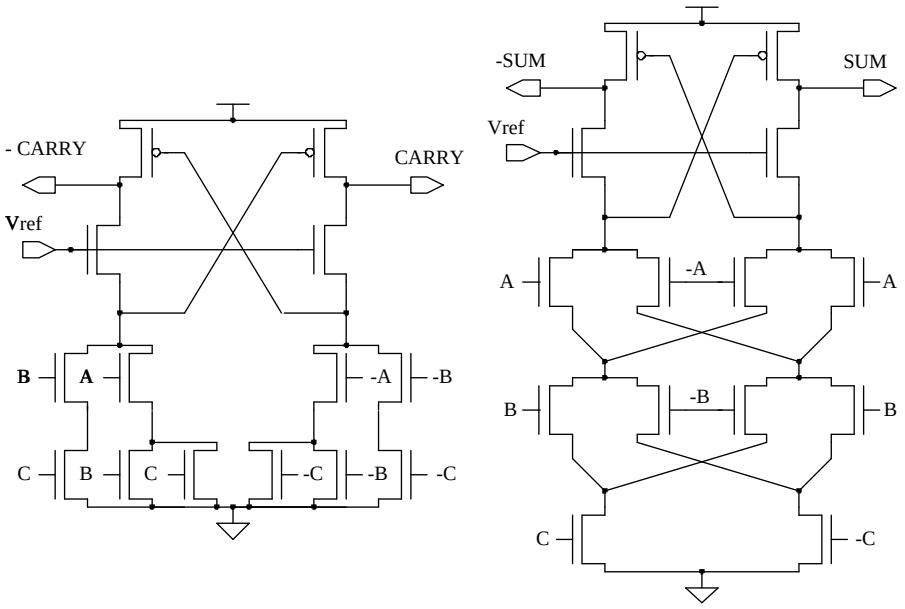

Figure 5.5. Static differential split-level full adder

5.3.6 Dual-Rail Domino Logic - DRDL

Dual-Rail Domino Logic [10,11] is a precharged circuit technique which is used to improve the speed of CMOS circuits. Figure 5.6 shows a Dual-Rail Domino full adder cell. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer. The dynamic circuit consists of a pMOSFET precharge transistor and an nMOSFET evaluation transistor with the clock signal (CLK) applied to their gate nodes, and an nMOSFET logic block which implements the required logic function. During the precharge phase (CLK = 0) the output node of the dynamic circuit is charged through the precharged pMOSFET transistor to the supply voltage level. The output of the static buffer is discharged to ground. During the evaluation phase (CLK = 1) the evaluation nMOSFET transistor is *ON*, and depending on the logic performed by the nMOSFET logic block, the output of the dynamic circuit is either discharged or it will stay precharged. Since in dynamic logic every output node must be precharged every clock cycle, some nodes are precharged only to be immediately discharged again as the node is evaluated, leading to higher switching power dissipation [1]. One major advantage of the dynamic, precharged design styles over the static styles is that they eliminate the spurious transitions and the corresponding power dissipation. Also, dynamic logic does not suffers from short-circuit currents which flow in static circuits when a direct

path from power supply to ground is caused. However, in dynamic circuits, additional power is dissipated by the distribution network and the drivers of the clock signal.

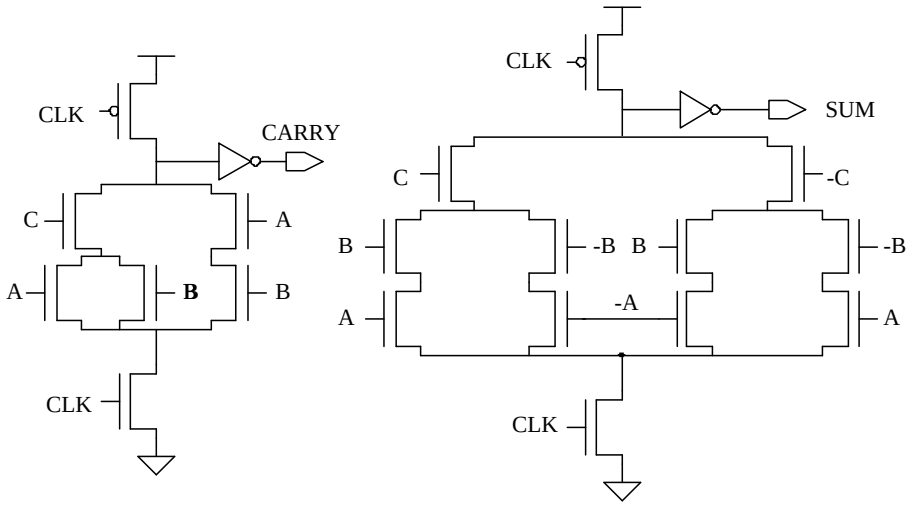

Figure 5.6. Dual-rail domino full adder

5.3.7 Dynamic Differential Cascode Voltage Switch Logic - DDCVSL

Dynamic DCVSL [8], is a combination between the domino logic and the static DCVSL. The circuit diagram of the dynamic DCVSL full adder is given in Figure 5.7. The advantage of this style over domino logic is the ability to generate any logic function. Domino logic can only generate noninverted forms of logic. For example, in the design of a ripple carry adder, two cells must be designed for the carry propagation, one for the true carry signal and another for the complementary one (in Figure 5.6, the cell for the true carry signal is only shown, but the one for the complementary signal is also required). Using DCVSL to design dynamic circuits will eliminate p-logic gates because of the inherent availability of complementary signals. The p-logic gates usually cause long delay times and consumes large areas.

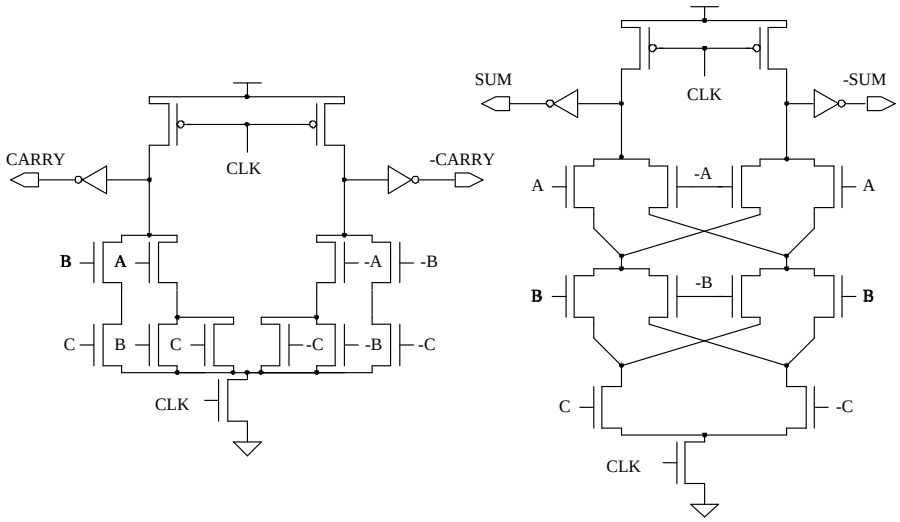

Figure 5.7. Dynamic differential cascode voltage switch full adder

5.3.8 Enable/disabled CMOS Differential Logic- ECDL

ECDL [12] is a self-timed differential logic which is used in the case of implementing logic functions using iterative networks. It uses extra signals to indicate the beginning and ending of a function evaluation, in order to improve the circuit speed. The structure of the ECDL full adder is illustrated in Figure 5.8. The signals Done_{i-1} and Done_i are the input and output self-timing control signals. During the disabled state, Done_{i-1} has a value of logic one, which discharges both the true and the complementary outputs to logic zero. During the enabled state, Done_{i-1} changes to logic zero and the topmost pMOSFET transistor (Figure 5.8) is *ON* to provide power to the inverters below. Then, depending on the logic of the differential nMOSFET network, a path exists from one of the output nodes to ground, holding that node to ground while leaving the other output node to be driven to logic one. One major advantage of the ECDL circuits is that there is no minimum clocking frequency requirement. However, ECDL circuits suffer from extra power dissipation due to the inverters which are needed to change the polarity of the output nodes. Also, their complex pull-up circuitry leads in extra silicon area.

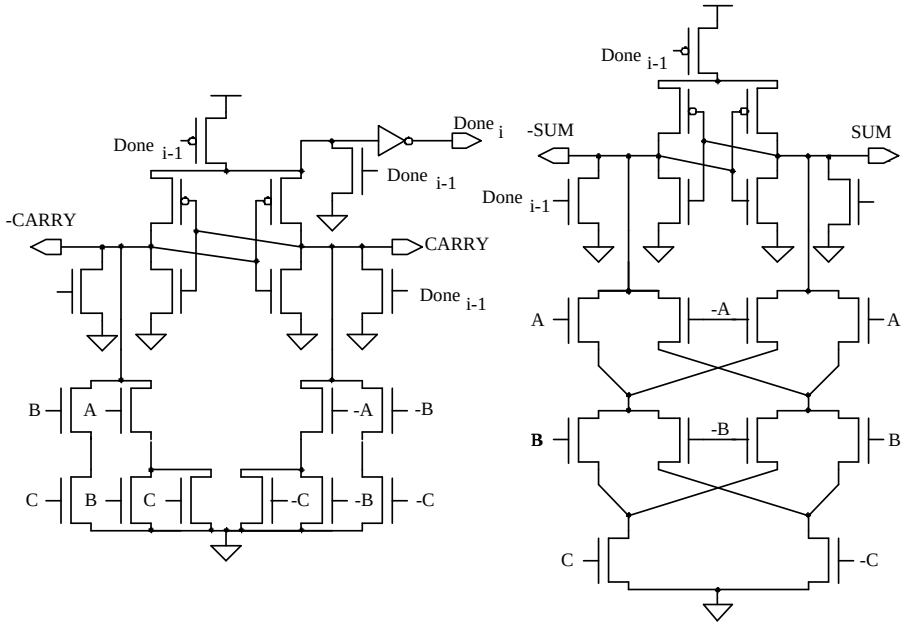

Figure 5.8. Enable/Disable CMOS differential full adder

5.4 Power, Delay and Area Comparisons of a 4-Bit Ripple Carry Adder

The experimental results described in this section were obtained using a four-bit ripple carry adder. A general block diagram of the adder is illustrated in Figure 5.9.

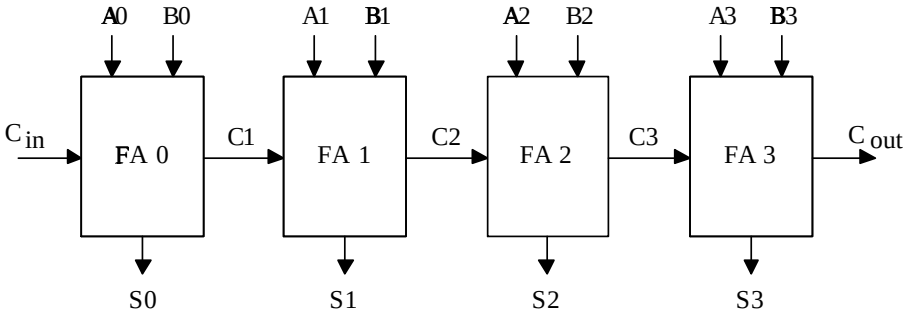

Figure 5.9. Block diagram of the four-bit ripple carry adder

The circuit was designed in a full custom manner for all the design styles described in the previous section, using a 1.5μm CMOS process technology. The channel width of the transistors was 4.8μm for the nMOSFETs, and 9.6μm for the pMOSFETs. The design was based on the full adder cells presented in Figures 5.1 to 5.8.

Figure 5.10 shows the layout of the conventional static four-bit ripple carry adder, as an example of the designed circuits.

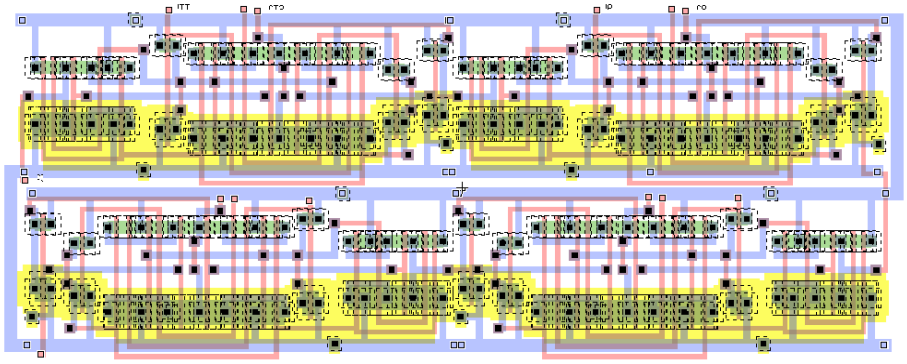

Figure 5.10. Layout of the conventional static four-bit ripple carry adder

In Table 5.1 the adder silicon area and the number of the transistors for each design style are given. Although no extensive attempts were made to minimize area, the numbers presented are a good indication of the relative areas of the eight adder implementations, which account not only for the transistors, but for the interconnections as well. For example, even though DPL adder has fewer transistors than the CSL one, it has longer interconnections, which is reflected by its large area. Dynamic design styles and styles which uses control signals (such as ECDL) occupy extra area for the routing of the clock and the control signals. The smallest area is occupied by the CPL circuit, which has fewer transistors and shorter interconnections than the other adder implementations.

After the design of the layouts, circuit equivalents were extracted for a detailed circuit simulation using HSPICE [2] to obtain the power and delay measurements. In our experiments, a supply voltage of 5Volts is used. All measurements were obtained with each input supplied through a driver consisting of two minimum-sized inverters in series, and each output node driving a minimum-sized inverter load.

The estimation of power dissipation is a difficult problem because of its data dependency, and has received a lot of attention [17]. Some direct simulative power estimation methods have been proposed [18,19], which are expensive in

Table 5.1. Area and number of transistors of the four-bit ripple carry adder implementations

Design Style	**Adder Area ($\times 10^4$ μm^2)**	**No. of Transistors**
CSL	5.42	144
CPL	4.46	88
DPL	6.52	136
SDCVSL	5.19	114
SDSL	6.39	130
DRDL	6.48	146
DDCVSL	7.22	154
ECDL	7.65	166

terms of time. Also, several power estimation methods have been proposed, where possibilities are used to solve the pattern-dependence problem. However, in order to achieve good accuracy, the spatial and temporal correlations between internal nodes should be modeled [20,21]. An alternative way is the use of statistical methods [22,23,17], that combines the accuracy of simulation-based techniques with the speed of probabilistic approaches.

In this chapter, the statistical approach proposed by Burch *et al.* [22] is used in order to estimate the power dissipation of our designs. Using the powermeter sub-circuit proposed by Kang [18], HSPICE can measure the average power consumed by a circuit given a set of input transitions and a time interval. In the method, the inputs are randomly generated and statistical mean estimation techniques are used to determine the final result. In our case for each adder design we use 200 independent, pseudorandom input transition samples, and the power consumed for each sample is monitored by HSPICE. All

simulations were carried out at 27˚C, with an input frequency of 50MHz in order to accommodate the slowest adder. The power dissipation measures do not include the power consumed by the drivers and the loads. In Figure 5.11, the probability distributions of the power dissipation per addition derived from the measurements, for the eight adder implementations, are shown. Since the data inputs are independent, power can be approximated to be normally distributed [22]. This conclusion can also be extracted from the curves of Figure 5.11.

Hence, the mean power dissipation is given by

$$\bar{P} \pm t_{\alpha/2}\frac{s}{\sqrt{N}}, \tag{5.4}$$

where $\bar{P}$ is the sample average, s is the standard deviation, N is the number of samples, and $t_{\alpha/2}$ is obtained from the $t-$distribution for a (1-α)% confidence

interval [24]. The mean power dissipation of the eight adder implementations using the simulation results and the equation (4) is given in Table 5.2.

The number of the required samples is extracted using the stopping criterion [22] of the above method

$$\frac{t_{\alpha/2}\, s}{\bar{P}\sqrt{N}} \quad < \quad e, \tag{5.5}$$

where e is the desired percentage error in the power estimate. The error in our statistical power analysis for N= 200 and 95% confidence interval ($t_{\alpha/2}$= 1.96) is less than 7%. In Table 5.2, the percentage error for each adder design is also given. For the four last designs the error is quite small because of the high normality of their distributions which leads to small standard deviation.

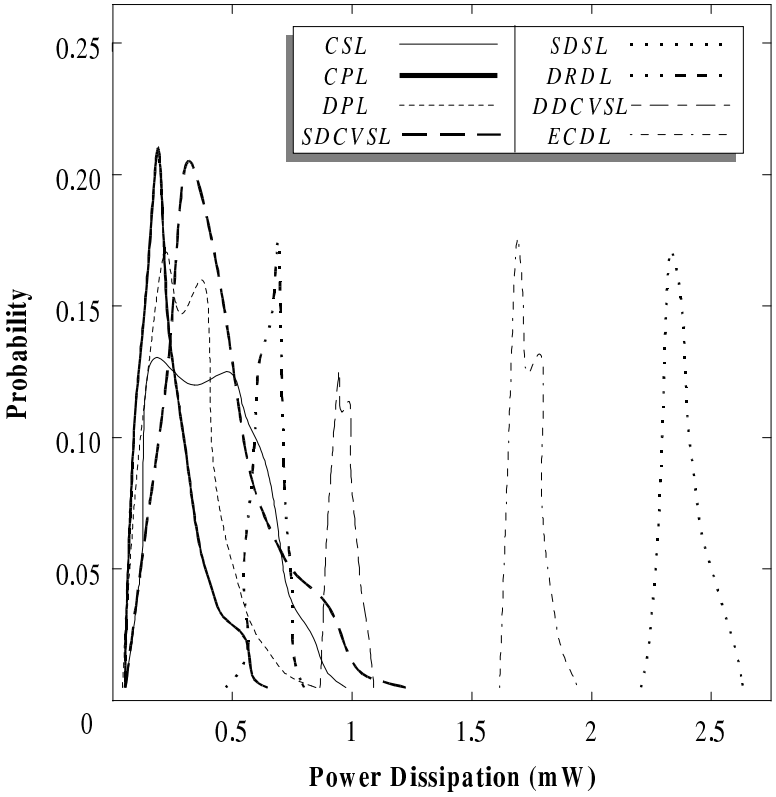

Figure 5.11. Power dissipation histograms

The delay of each design was measured directly from the output waveforms generated by simulating the adder using HSPICE for the worst case inputs, that is, inputs which cause the carry to ripple from the least significant bit position to most significant bit position. The worst case delays of the eight adder designs are listed in the fourth column of Table 5.2. As mentioned in Section 5.1, the most essential metric of performance in modern VLSI applications is the power-delay product. By multiplying each power measurement with the worst case delay, we can found the mean power-delay product of the designs using a method similar to that used for the mean power dissipation. Hence, the mean power-delay product is given by

$$\overline{P \times D} \pm t_{\alpha/2}\frac{s}{\sqrt{N}}, \tag{5.6}$$

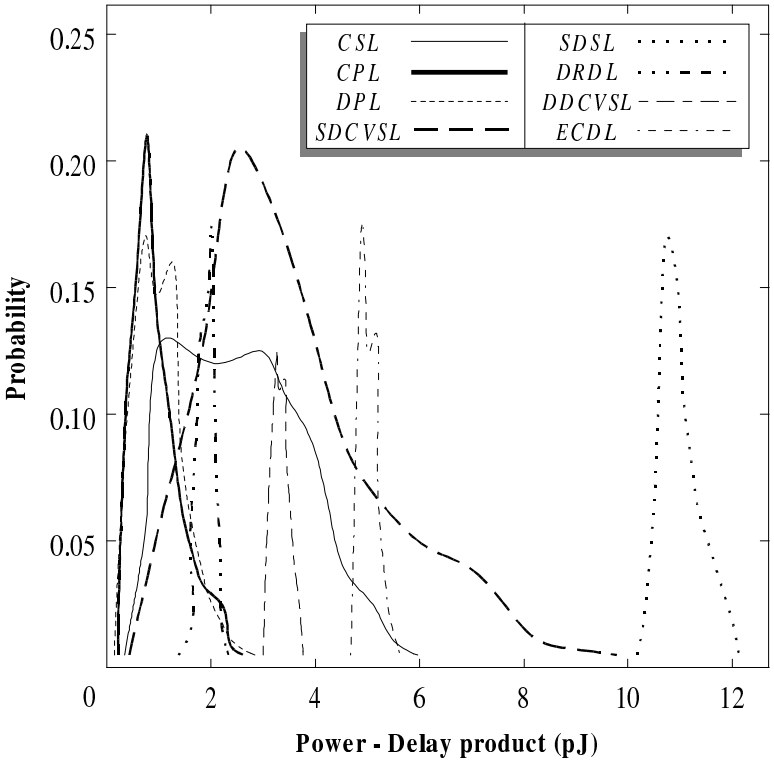

Figure 5.12. Power-delay product histograms

where $\overline{P \times D}$ is the sample average power-delay product. The mean power-delay product values of the eight adder designs are listed in Table 5.2, and the probability distributions of the power-delay product are shown in Figure 5.12.

Table 5.2. Power dissipation, delay and power-delay product of the four- bit ripple carry adder implementations

Adder Design Style	**Mean Power Dissipation per addition (**mW**)**	**Statist. Error (%)**	**Worst Case Delay (**nsec**)**	**Mean Power-Delay Product per addition (**pJ**)**
CSL	0.422 ± 0.0302	6.1	6.125	2.585 ± 0.1850
CPL	0.238 ± 0.0208	4.8	4.042	0.962 ± 0.0841
DPL	0.305 ± 0.0263	6.9	3.345	1.020 ± 0.0879
SDCVSL	0.432 ± 0.0362	6.5	7.986	3.450 ± 0.2891
SDSL	2.383 ± 0.0129	0.6	4.606	10.976 ± 0.0594
DRDL	0.641 ± 0.0091	1.4	2.909	1.865 ± 0.0265
DDCVSL	0.957 ± 0.0074	0.8	3.453	3.304 ± 0.0255
ECDL	1.721 ± 0.0096	0.6	2.892	4.977 ± 0.0278

As we can see in the probability distributions of Figure 5.12, the curves of the dynamic designs (DRDL and DDCVSL) are shifted to the right, because of the power dissipated due to the precharge cycles. The same phenomenon occurs in the ECDL adder due to the power dissipation of its disabled state. The shifting to the right of the SDSL adder curve is caused because of the high static power which is dissipated due to the incomplete turn-off of the cross-coupled pMOSFET transistors. The other static design styles are more power efficient compared to the dynamic circuits.

The static DCVSL circuit consumes more power than the conventional static circuit due to the difference of the charging and discharging times of its output nodes. The asymmetry in the rise and fall times of the potential at these output nodes will prolong the period of current flow through the latch during the transient state, thus increasing the power dissipation.

It can be obtained from the results of Table 5.2, that the dynamic circuits exhibit an increase in speed compared to the conventional static circuit. Comparing the dynamic logic styles, Domino logic has better power-delay product characteristics (Figure 5.12). The circuit operation in the SDSL circuit becomes faster than the standard SDCVSL circuit, due to the reduced logic swing at the output nodes, but in the cost of high static power dissipation. ECDL circuit is the faster one, but consumes high switching power due to the inverters which are needed to change the polarity of the outputs.

The design styles which use pass-transistor logic (CPL and DPL) are the best in terms of power dissipation. CPL circuit consumes lower power than the DPL one, because of its lower parasitic capacitance. On the contrary, DPL circuit is

faster than the CPL, because the addition of pMOSFET transistors in parallel with the nMOSFET transistors results in higher circuit drivability. Also, DPL avoids the problems of noise margin and speed degradation at reduced supply voltages which are caused in CPL circuits. As shown in Figure 5.12 and in Table 5.2, the two styles exhibit similar power-delay product characteristics, and they are the most efficient for low-power and high-speed applications.

The mean power dissipation and the propagation delay values of the eight adder implementations are summarized in Figure 5.13. The fast adder circuits lie to the left of the figure , and those with low power consumption lie toward the bottom of the figure .

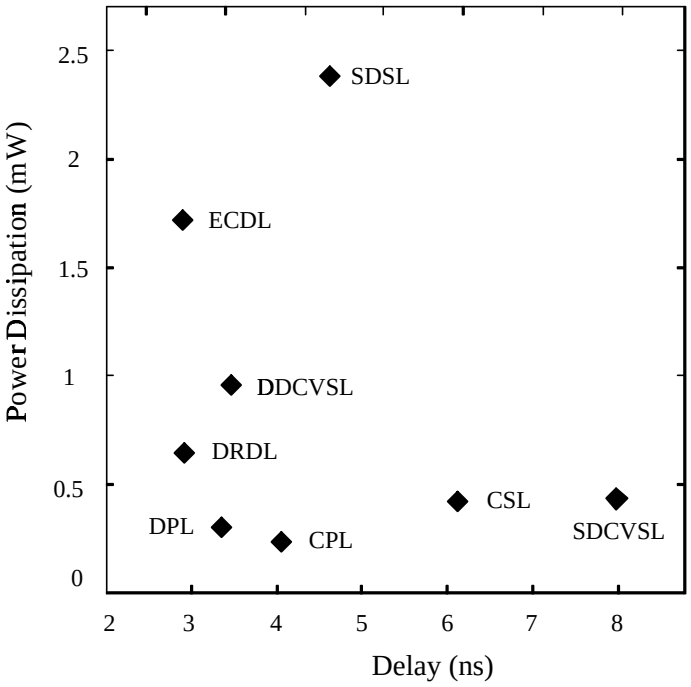

Figure 5.13. Power dissipation versus delay of the adder implementations

5.5 Adders

In static CMOS the dynamic power dissipation of a circuit depends primary on the number of transitions per unit area. As a result, the average number of logic transitions per addition can serve as the basis of comparing the efficiency of a variety of adder designs. If two adders require roughly the same amount of time and roughly the same number of gates, the circuit which requires fewer

logic transitions is more desirable as it will require less dynamic power. This is only a first order approximation as the power also depends on switching speed, gate size, fan-out, output loading e.t.c.

The following types of adders were simulated: Ripple Carry, Constant Block Width Single-level Carry Skip, Variable Block Width Multi-level Carry skip, Carry Lookahead, Carry Select, and Conditional Sum. Table 5.3 presents the worst case number of gate delays, the number of gates, and the average number of logic transitions for the six 16-bit adder types. All the gates are assumed to have the same delay, regardless of the fan-in or fan-out.

Table 5.3. Worst Case Delay, Number of Gates, and Average Number of Logic Transitions for a 16-bit Adder

Adder Type	**Worst Case Delay (in gates units)**	**Number of Gates**	**Average Number of logic Transitions**
Ripple Carry	36	144	90
Constant Block Width Single-level Carry Skip	23	156	102
Variable Block Width Multi-level Carry skip	17	170	108
Carry Lookahead	10	200	100
Carry Select	14	284	161
Conditional Sum	12	368	218

5.6 Multipliers

The majority of the real life applications, such as microprocessors and digital processing implementations, require the computation of the multiplication operation. Specifically, speed, area and power efficient implementation of a multiplier is a very challenging problem. Here, four well-known multipliers: i) the Array Multiplier [25], ii) the Split Array Multiplier [26], iii) Wallace Tree Multiplier [27] and iv) the Radix-4 Modified Booth Recoded Wallace Tree Multipliers [28], are studied in terms of power consumption.

Two kinds of measurements and comparisons in the terms of different design parameters are performed providing to the designer a plethora of alternative implementations. Particularly, we provide SPICE-like measurements with respect to the average logic transitions as well as the power consumption. The second

kind of measurements are performed following a typical high-level analysis flow and is based on a state-of-the-art CAD framework.

5.6.1 SPICE-like Power Measurements of Multipliers

The multipliers were described using only AND, OR, and INVERT gates. The simulation was made using a program called CazM [29], which is similar to SPICE. Each multiplier was fed with 1.000 pseudorandom inputs. For the sake of completeness, the carry save array multiplier and the Wallace tree is presented in the following section, in order to briefly describe the architectures of the most common multipliers. The former is a representative paradigm of array multipliers, while the Wallace tree is an efficient way to add multiple partial products together.

A gate level simulation with 10.000 pseudorandom inputs, enabled the gathering of average number of gate-output transitions for each multiplier. During each input, the number of gates that switch output states is recorded, and an average number of gate-output transitions per multiplication are computed at the end of the simulation. Table 5.4 presents the results.

Table 5.4. Average Number of Gate-Output Transistions

	Average Number of Gate-Output Transitions		
Multiplier Type	**8-bit**	**16-bit**	**32-bit**
Array	570	7224	99906
Split array	569	4874	52221
Wallace	549	3793	20055
Modified booth	964	3993	19542

The average power dissipation per multiplication is shown in Table 5.5. These results were obtained by simulating the multiplication of 1000 pseudorandom inputs with a clock period of 100 ns. The results vary significantly. The Wallace multiplier, which presents the lower power dissipation, is neither the smallest nor the slowest one.

5.6.2 High-Level Power Characterization of Multipliers

The second power estimation procedure is illustrated in Figure 5.14.The first step is the logic synthesis of the parameterized and structural VHDL description of the arithmetic modules. Here, a 0.6-micron process, AMS standard-cell library has been used. For power characterization, only the dynamic power dissipation, which forms the dominant component of the total power, is taken

Table 5.5. Avarage Power Dissipation from CAzM

Multiplier Type	Power (mW)	Logic Transitions
Array	43.5	7224
Split array	38.0	4874
Wallace	32.0	3793
Modified booth	41.3	3993

into account [30]. Specifically, the activity per node, resulting via logic-level simulation that takes place in a second step, is combined with the capacitance per node, to compute the power for a certain input vector, according to

$$Power = \sum_{i=1}^{N} C_{load_i} \; V_{dd}^2 \, f \, E_i \tag{5.7}$$

where C_{load_i} is the capacitance at node i, V_{dd} is the power supply voltage , f is the frequency and E_i is the activity factor at node i. The term $f \cdot E_i$ of Eq. 5.7 is actually the number of transitions from logic '1' to logic '0' per time unit for the node i, which is equal to the ratio of number of node transitions from logic '1' to logic '0', divided by the total number of input vectors:

$$f \cdot E_i = f_{1\rightarrow 0} = \frac{\#trans_{1\rightarrow 0_i}}{\#vectors} \tag{5.8}$$

From Eq. 5.7 and 5.8, the power is:

$$Power = \frac{V_{DD}^2}{\#vectors} \sum_{i=1}^{N} C_{load_i} \#trans_{1\rightarrow 0_i} \tag{5.9}$$

Following this procedure, the power estimation errors are in the range of 10-25% [31], compared with SPICE transistor-level simulator. However, the accuracy of the estimates suffices for the purpose of comparing alternative module architectures, since its relative evaluation is of importance and not the absolute accuracy. The 8-bit wide input modules were simulated with 50.000 random vectors, the 16-bit modules with 100.000 vectors, the 32-bit modules with 150.000 random vectors, and the 64-bit modules with 200.000 vectors. It should be stressed here, that the energy figures, given later in the characterization sections of the arithmetic components, correspond to the average energy per operation. The difference of the two characterization procedures in the number of test vectors is significant.In this section, power measures for the synthesized multipliers, namely the carry save array, the Booth encoded Wallace tree and

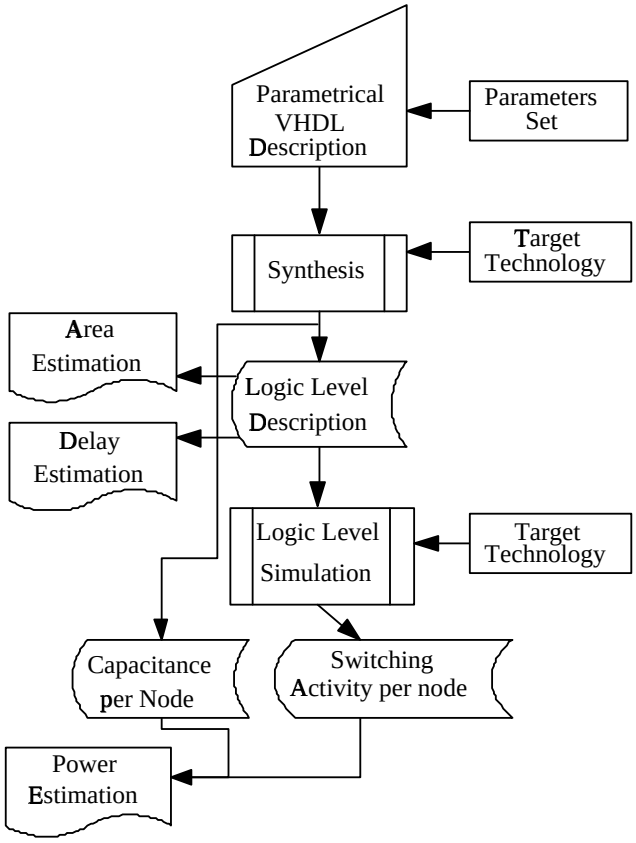

Figure 5.14. High level Characterization Flow

the non-Booth encoded Wallace tree, will be presented, while analysis of results and comparisons with previous work are made.

Table 5.6 presents the power estimation of the synthesized multipliers. The measurements of power are normalized by frequency, reflecting the fact of simulation, with different operating frequencies. In this way, a representative power measure is given, for every kind of multiplier and for every bit width. As it is shown in Table 5.6, the most power-efficient multiplier for small bit-widths (less than 32 bits) is the carry save array, but with a small difference, compared to the Wallace tree with non-Booth encoding. In the 64-bit implementations, the Wallace tree with non-Booth encoding multiplier is the most power efficient choice. This fact is explained by the glitches arising from the ripple of carries of the array multiplier for large bit-widths. Finally, for all bit-widths, the Wallace tree with Booth encoding multiplier has the worst power dissipation.

Table 5.6. Power dissipation estimates

	Power (mW)			
Multiplier Type/ Multiplier Width	**8-bit**	**16-bit**	**32-bit**	**64-bit**
Carry Save Array	0.3084	2.2484	3.057023	20.96759
Wallace Tree (Booth Encoded)	0.7868	3.1204	5.384	23.7164
Wallace Tree (Non Booth Encoded)	0.5488	2.5992	4.2212	18.8588

For comparison purposes, Table 5.7 shows the results presented in [29], considering 16-bit implementations of array and Wallace tree multipliers. These designs were described only by AND, OR, and INVERT gates. The implementation technology was a 2-level metal 2-μm process. It can be seen that the array multiplier consumes more energy than the Wallace tree multiplier, which is contradictory to corresponding values shown in Table 5.6. Only in the 64-bit case, the array multiplier consumes more energy than the Wallace tree multiplier. The reason for this is the spurious transitions that occur by the rippling of carries for the array multiplier of the 64-bit implementation, which cannot compensate the interconnect area/capacitance switched by the array multiplier. For the remaining cases, the factors of the greater interconnect and cell area for the Wallace multiplier dominate the power performance of these two kinds of multipliers.

Table 5.7. 16-bit Multiplier Average Power Dissipation [29]

Multiplier	**Power (mW)**	**Logic transitions**
Carry Save Array	43.5	7224
Wallace Tree	32	3793

The Wallace multiplier with Booth encoding dissipates the most power, while it is not the largest. It is the fastest multiplier for bit-widths larger than 16 bits and can be assumed that Booth encoding is a rather power-hungry operation.

Finally, Table 5.8 depicts the *Power*×*Delay product* of the multipliers at 1MHz frequency. More specifically, the carry save array multiplier exhibits the worst product for all bit-widths, except the 8-bit, due to the large delay and the substantial power consumption Although the non-Booth Wallace tree multiplier is the largest, it shows the best *Power*×*Delay product* for every bit-width. Where speed is of great interest, especially if large bit widths are required, and chip area is not a problem, the non-Booth encoded Wallace tree multiplier is the best candidate for selection.

Table 5.8. Power-Delay product of Multipliers at 1MHz

	Power*Delay (mW*ns)			
Multiplier Type/ Multiplier Width	**8-bit**	**16-bit**	**32-bit**	**64-bit**
Carry Save Array	4,13256	53,51192	141,9987	2090,049
Wallace Tree (Booth Encoded)	4,980444	25,96173	58,09336	312,345
Wallace Tree (Non Booth Encoded)	3,172064	19,8059	44,95578	251,9536

5.7 Conclusions

In this chapter, the most common kinds of adders and multipliers have been characterized in terms of power, using either a traditional low-level design flow paradigm, which is rather tedious and incompatible with modern design flows, but provides the most accurate results, or a high-level design flow paradigm, which is commonly used.

A four-bit ripple carry adder was used, as the benchmark circuit. All the circuits have been designed in a full-custom manner, and simulated using HSPICE. A statistical approach was used in order to analyze the simulation results. It has been shown that the circuits which use pass-transistor logic (CPL and DPL) exhibit better power and the power-delay product characteristics compared to other design styles.

The array multiplier is power-efficient for small bit widths. Its power consumption grows in proportion to the cube of the word size. The Wallace multiplier is less regular, but is more power efficient, while its power dissipation grows with the square of the word size.

The speed of the synthesized optimized carry look-ahead is traded-off for the worst energy power consumption among all the investigated adders, which have been synthesized. As opposed to the speed optimized architecture of the carry look-ahead adder, a non-optimized architecture is power-efficient, though much slower. Power-efficient is the ripple carry adder, too.

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