Short-Circuit Energy Dissipation Modeling for Submicrometer CMOS Gates

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***Abstract*—A significant part of the energy dissipation in static complementary metal–oxide-semiconductor (CMOS) structures is due to short-circuit currents. In this paper, an accurate analytical model for the CMOS short-circuit energy dissipation is presented. First, the short-circuit energy dissipation of the CMOS inverter is modeled. The derived model is based on analytical expressions of the inverter output waveform which include the influences of both transistor currents and the gate-to-drain coupling capacitance. Also, the effect of the short-circuiting transistor's gate-source capacitance on the short-circuit energy dissipation, is taken into account. The α-power law MOS model that considers the carriers' velocity saturation effect of submicrometer devices is used. Second, the inverter model is extended to static CMOS gates by using reduction techniques of series- and parallel-connected transistors. The results produced by the suggested model for a commercial 0.8-μm process, show very good agreement with SPICE simulations.**

***Index Terms*—CMOS gates, circuit modeling, circuit simulation, inverters, short-circuit power dissipation, submicrometer MOSFETs.**

I. Introduction

SINCE energy dissipation is one of the most critical design parameters in very large scale integration (VLSI) circuits, accurate and efficient energy evaluation during the design phase is required, in order to meet the desired specifications without a costly redesign process. Energy dissipation in complementary metal–oxide–semiconductor (CMOS) circuits consists mainly of two parts, the capacitive and the short-circuit dissipation [1]. Capacitive dissipation caused by charging and discharging the load capacitance of a CMOS structure, is well understood and easy to be estimated. During switching in a static CMOS gate, a direct path from the power supply to the ground is established, resulting in short-circuit energy dissipation.

The first goal of this work is the analytical evaluation of short-circuit energy dissipation in CMOS inverters. The first closed-form expression for the evaluation of the short-circuit energy dissipation in a CMOS inverter was presented by Veendrick [2], where zero-load capacitance and current waveform which is mirror symmetric about a central vertical axis (at the half of the input transition time) were assumed. This expression gives pessimistic results mainly due to the assumption of zero-load capacitance, and is based on the Shichman and Hodges [3] square-law MOS model that ignores the carriers' velocity saturation effects of submicrometer devices. In [4] and [5], an expression without the simplifications of [2] was derived. However, the square-law MOS model was still used and the expression of the output waveform was derived with negligible short-circuit current. Recently, a similar model was proposed in [6]. In this, two fitting parameters are inserted to the expression of the output waveform derived in [4], in order to include the reaction of the short-circuiting transistor to the output charge or discharge operation. In [7], an inverter short-circuit energy dissipation model, which is still based on the square-law MOS model, was presented. It includes the influences of the short-circuit current and the gate-to-drain coupling capacitance on the inverter output waveform. In [8], the short-circuit energy dissipation is evaluated through an equivalent short-circuit capacitance. The derived average short-circuit current depends on the ratio between the output and the input transition times of the inverter. However, as mentioned in [6], in the cases where this ratio is lower than 3, the average current may exceed the maximum average short-circuit current obtained in [2] for zero-load capacitance.

In order to develop simple yet accurate short-circuit energy dissipation models for modern submicrometer technologies, simple and efficient MOS models [9]–[10] including the carriers' velocity saturation effect of submicrometer devices, have been used. Sakurai and Newton [9] presented a formula for the short-circuit energy dissipation, which is a direct extension of the formula presented in [2]. The only difference is the use of the α-power MOS model for the saturation current expression instead of the square-law MOS model, while all the assumptions of [2] are retained. Vemuru and Scheinberg [11] proposed a formula for the evaluation of the short-circuit power dissipation based on the α-power MOS model, where the analytical expression of the output waveform does not include the influences of the short-circuit current and the gate-to-drain coupling capacitance. Also, it was assumed that the load transistor operates only in the saturation region during the time when short-circuit current flows.

In [12], the short-circuit current waveform was approximated with a piecewise linear function of time, in order to estimate the short-circuit energy dissipation. However, the energy of the reverse current due to the gate-to-drain coupling capacitance is subtracted from the short-circuit energy dissipation. This reverse current is provided from the inverter input (or the supply of the previous gate), so its energy component cannot be included to the short-circuit energy dissipation, which is due to the direct current from the power supply to the ground. Recently, in [13] a short-circuit energy macromodel for the CMOS inverter

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was proposed, which uses a simple MOS model [14] for submicrometer devices. In this, the short-circuit energy dissipation is evaluated through a fictitious short-circuit capacitance. The inverter output is approximated by a linear waveform, based on the inverter propagation delay which is calculated [15] using the empirical timing model proposed in [16] and [17]. Also, during the short-circuit part of the transition, the charge through the short-circuiting transistor is assumed to be the same in linear and saturation regions.

In this paper, an analytical expression for the evaluation of the short-circuit energy dissipation in a CMOS inverter, based on the α-power law MOS model [9], is derived. For the derivation, analytical expressions of the output waveform in the operation regions which are required for the evaluation of the short-circuit energy dissipation, are used. These expressions take into account the current through both transistors. In order to obtain better accuracy, avoiding an overestimation of the short-circuit energy dissipation, we consider the influence of the input-to-output coupling capacitance (gate-drain capacitance of both transistors) and the short-circuiting transistor's gate-source capacitance. The derived model is more accurate and efficient than that proposed in our previous work [18], where a less accurate and simpler MOS model [14] was used.

The importance of modeling the inverter comes from the fact that a great fraction of the energy dissipated in CMOS VLSI circuits is due to the clock driving circuits and I–O drivers (pads), which are based on inverters. In a system designed with static logic, the clock driving power reaches 40% of the total power (excluding the off-chip driving power), while the logic circuit power is lower than 20% [19]. Moreover, the power dissipated in off-chip drivers (pads) could be more than 15% of the total chip power [19]. Another equally important reason to have an accurate model for the inverter short-circuit energy dissipation, is that several fast methods for reducing a CMOS gate to an equivalent inverter have been proposed [20]–[22]. For the extension of the proposed inverter model to static CMOS gates, the series-connected transistors, when operated as a charging or discharging block, are reduced to an equivalent transistor using the method proposed in our previous work [22]. Also, a reduction technique for the case where the series-connected transistors operate as short-circuiting block is proposed. The channel width of the equivalent transistor in the case of parallel-connected transistors is extracted by adding the widths of the switching transistors.

The rest of the paper is organized as follows. In Section II, our method for the evaluation of the inverter short-circuit energy dissipation is presented. The extension of the proposed inverter model to static CMOS gates is discussed in Section III. Results and comparisons with previous works and SPICE measurements are given and discussed in Section IV. Finally, we conclude in Section V.

II. Short-Circuit Energy Dissipation of the CMOS Inverter

The derivations presented in the following are for a rising input ramp: $V_{\rm in} = V_{\rm DD} \cdot (t/\tau)$ for $0 \le t \le \tau, V_{\rm in} = 0$ for $t \le 0$ and $V_{\rm in} = V_{\rm DD}$ for $t \ge \tau$, where τ is the input rise time. The analysis for a falling input is symmetrical. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter (Fig. 1), taking into account the current through the gate-to-drain coupling capacitance (C_M) is written as

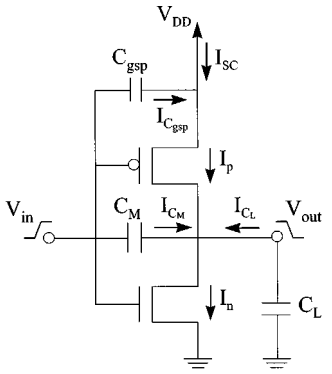

Fig. 1. The CMOS inverter.

$$C_L \frac{dV_{\rm out}}{dt} = C_M \left(\frac{dV_{\rm in}}{dt} - \frac{dV_{\rm out}}{dt} \right) + I_p - I_n. \qquad (1)$$

The output load C_L consists of the inverter drain junction capacitances, the gate capacitances of fan-out gates, and the interconnect capacitance. The equivalent gate-drain capacitance C_M is the sum of the gate-to-drain capacitances of both transistors, which consists of the gate-to-drain overlap capacitance and a part of the gate-to-channel capacitance. It is calculated using the parameters $C_{\rm ox}$ (gate-oxide capacitance per unit area) and $C_{\rm gdo}$ (gate-drain overlap capacitance per unit channel width) [23].

For the expressions of the transistor currents the four-parameter α-power law MOS model [9] is used. The parameters are the velocity saturation index (α), the drain current (I_{D0}) at $V_{\rm GS} = V_{\rm DS} = V_{\rm DD}$, the drain saturation voltage (V_{D0}) at $V_{\rm GS} = V_{\rm DD}$ and the threshold voltage $(V_{\rm TH})$. After normalizing voltages with respect to the supply voltage $(V_{\rm DD})$, i.e., $u_{\rm in} = V_{\rm in}/V_{\rm DD}, u_{\rm out} = V_{\rm out}/V_{\rm DD}, n = V_{{\rm TH}n}/V_{\rm DD}, p = |V_{{\rm TH}p}|/V_{\rm DD}, u_{\rm don} = V_{D0n}/V_{\rm DD}, u_{\rm dop} = |V_{D0p}|/V_{\rm DD}$ and using the variable $x = t/\tau$, the PMOS device current is given by the following equation:

$$I_p = \begin{cases} k_{\rm lp}(1-x-p)^{\alpha_p/2}(1-u_{\rm out}), \\ \qquad 1-u_{\rm out} < u'_{\rm dop}, \text{ Linear region} \\ k_{\rm sp}(1-x-p)^{\alpha_p}, \\ \qquad 1-u_{\rm out} \ge u'_{\rm dop}, \text{ Saturation region} \\ 0, \qquad x \ge 1-p, \text{ Cutoff region} \end{cases} \qquad (2)$$

where

$$k_{\rm sp} = \frac{I_{D0p}}{(1-p)^{\alpha_p}}, \quad k_{lp} = \frac{I_{D0p}}{u_{\rm dop}(1-p)^{\alpha_p/2}}$$

$$u'_{\rm dop} = u_{\rm dop} \left(\frac{1-x-p}{1-p} \right)^{\frac{\alpha_p}{2}}$$

and the NMOS device current in a similar way.

For the evaluation of the short-circuit energy dissipation, analytical expressions of the output waveforms in the two first inverter operation regions (Fig. 2) are required. In region 1 $(0 \le$

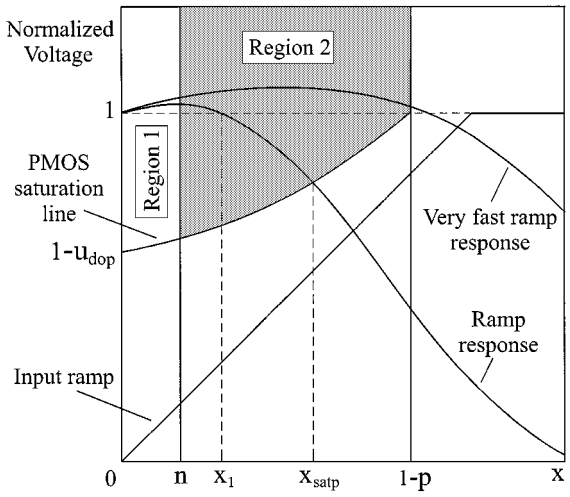

Fig. 2. Operation regions of the inverter.

$x \leq n$) the NMOS transistor is off and the PMOS transistor is in the linear region, while in region 2 ($n \leq x \leq x_{\text{sat}\,p}$) the NMOS transistor is saturated and the PMOS transistor is still in the linear region. $x_{\text{sat}\,p}$ is the normalized time value when the PMOS transistor is entering the saturation region. Part of the charge from the input which injected through the gate-to-drain coupling capacitance causes an overshoot at the early part of the output voltage waveform ($0 \leq x \leq x_1$). During the overshoot there is no current from power supply to ground because the output voltage is greater than the supply voltage. In the special case of very fast input ramps, the PMOS device is turned off after its linear region without enters saturation (Fig. 2). This occurs because the output voltage overshoot finishes when the PMOS device is already off. In this case there is no short-circuit energy dissipation.

The analytical expressions of the inverter output waveform in the above regions have been derived by solving the differential equation (1) (using some efficient approximations) in our previous work [24]. In region 1, the output voltage is expressed as

$$u_{\text{out}} = 1 + c_m y_n^{-1}(1 - e^{-y_n x}) \tag{3}$$

where

$$y_n = A_{lp}\left(1 - p - \frac{n}{2}\right)^{\alpha_p/2}$$

$$A_{lp} = \frac{k_{lp}\tau}{V_{\text{DD}}(C_L + C_M)}$$

and

$$c_m = \frac{C_M}{C_L + C_M}.$$

In region 2, the PMOS current is approximated by a linear function of the normalized time (Fig. 3): $I_p = I_{p\min} + S(x - n)$. $I_{p\min}$ is calculated using the PMOS current equation in the linear region and the value of the normalized output voltage at $x = n$ in (3). The current slope S is calculated by equating the exact PMOS current in the linear region [see (2)] with the approximated one, at the point $x_c = (1 - p)/2$. After that, the output voltage waveform is described by

$$u_{\text{out}} = 1 + c_m(x - n + R) + I_{p\min} d(x - n) + \frac{Sd(x-n)^2}{2} - \frac{A_{sn}(x-n)^{\alpha_n+1}}{\alpha_n + 1} \tag{4}$$

where

$$R = y_n^{-1}(1 - e^{-ny_n}), \quad d = \frac{\tau}{V_{\text{DD}}(C_L + C_M)}$$

and

$$A_{sn} = \frac{k_{sn}\tau}{V_{\text{DD}}(C_L + C_M)}.$$

The normalized time value $x_{\text{sat}\,p}$ satisfies the PMOS saturation condition: $u_{\text{out}} = 1 - u'_{\text{dop}}$. In order to solve this equation a Taylor series expansion around the point $x = 1 - p - n$ up to the second-order coefficient is used, for both u_{out} and u'_{dop}. The normalized time value x_1 where the output voltage overshoot finishes is calculated by the equation $u_{\text{out}} = 1$, using the Taylor series expansion of u_{out} around the point $x = 2n$. Equations (3) and (4) give waveforms very close to those derived from SPICE simulations (as shown in [24]). Note that, in [11] a rough approximation for $x_{\text{sat}\,p}$ is used ($x_{\text{sat}\,p} = 1 - p - n$). In [13], a linear output waveform and a constant u'_{dop} are used in order to calculate $x_{\text{sat}\,p}$, and the PMOS transistor current is neglected during the calculation of x_1. The above approximations of previous works result in important errors in the evaluation of the short-circuit energy dissipation.

The short-circuit energy dissipation in the case of rising input is the energy of the current (I_{SC}) provided from the power supply (Fig. 1). The inverse current which flows during the interval $[0, x_2]$ (Fig. 4) is due to the presence of the gate-drain coupling capacitance (C_M) and the gate-source capacitance of the PMOS transistor (C_{gsp}). The current through these capacitances is provided from the input (or the power supply of the previous gate) during its transition. As shown in Fig. 4, the current through C_{gsp} causes a decrease in the positive short-circuit current pulse resulting in reduced short-circuit energy dissipation.

The short-circuit energy dissipation during a falling output transition is defined as

$$E_{\text{SC}}^{1\to 0} = V_{\text{DD}} \int_{x_2}^{x_3} I_{\text{SC}}\tau\, dx = V_{\text{DD}} \left(\int_{x_2}^{x_{\text{sat}\,p}} I_{\text{SC}}\tau\, dx + \int_{x_{\text{sat}\,p}}^{x_3} I_{\text{SC}}\tau\, dx \right) \tag{5}$$

where $I_{\text{SC}} = I_p - I_{C_{\text{gsp}}}$.

The current through C_{gsp} during the input transition is given by

$$I_{C_{\text{gsp}}} = C_{\text{gsp}} \frac{dV_{\text{in}}}{dt} = C_{\text{gsp}} \frac{V_{\text{DD}}}{\tau}. \tag{6}$$

The value of C_{gsp} depends on the PMOS transistor operating mode, and is calculated using the parameters C_{ox} and C_{gso} (gate-source overlap capacitance per unit channel width) [23].

In the first integral of (5) a linear approximation of the PMOS transistor current is used (Fig. 4)

$$I_p = S'(x - x_1). \tag{7}$$

S' is the slope of I_p and is calculated by equating the exact PMOS current in the linear region [see (2)] with the approxi-

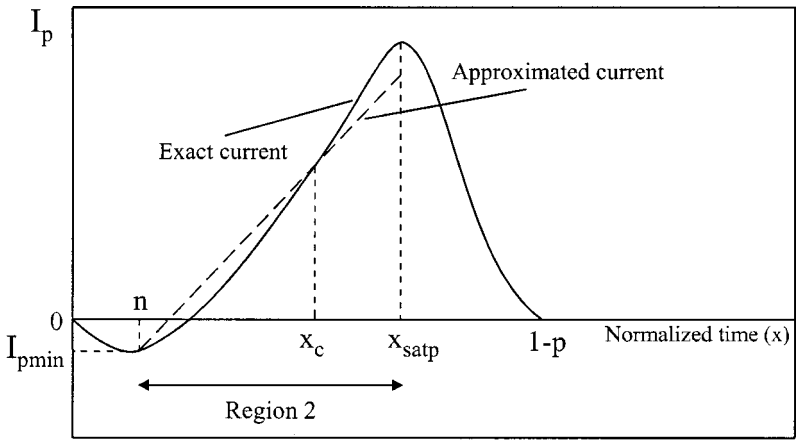

Fig. 3. Linear approximation of the PMOS current in region 2.

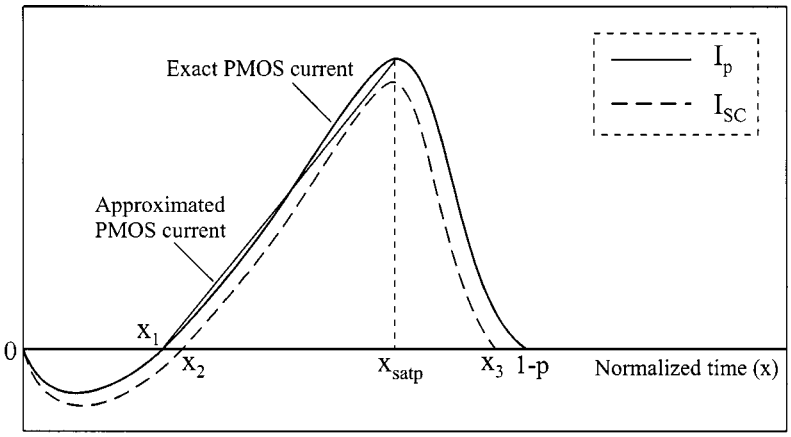

Fig. 4. PMOS and short-circuit current waveforms of the inverter.

mated one, at the middle of the interval $[x_1, x_{\text{sat}\,p}]$. In the second interval of (5), the PMOS current equation as given from the α-power MOS model [see (2)] for the saturation region, is used. After that, the short-circuit energy dissipation is given by the following expression:

$$E_{\text{SC}}^{1\to 0} = \frac{V_{\text{DD}}\tau}{2}(x_{\text{sat}\,p} - x_2) \times \left[(x_{\text{sat}\,p} + x_2 - 2x_1)S' - \frac{2C_{\text{gsp}}V_{\text{DD}}}{\tau}\right] + \frac{V_{\text{DD}}k_{\text{sp}}\tau}{(\alpha_p+1)}\left[(1-p-x_{\text{sat}\,p})^{\alpha_p+1} - (1-p-x_3)^{\alpha_p+1}\right] - C_{\text{gsp}}V_{\text{DD}}^2(x_3 - x_{\text{sat}\,p}). \quad (8)$$

The value x_2 is the normalized time point where the short-circuit current equals zero, and is easily calculated by the equation

$$S'(x_2 - x_1) - C_{\text{gsp}}(V_{\text{DD}}/\tau) = 0. \quad (9)$$

Similarly, the normalized time value x_3 is calculated by the following equation:

$$k_{\text{sp}}(1 - x - p)^{\alpha_p} - C_{\text{gsp}}(V_{\text{DD}}/\tau) = 0. \quad (10)$$

In order to solve (10), we use a Taylor series expansion of the term $k_{\text{sp}}(1-x-p)^{\alpha_p}$ around the point $x = [x_{\text{sat}\,p}+3(1-p)]/4$ up to the second-order coefficient.

The analysis for the evaluation of the short-circuit energy dissipation during the rising output transition is symmetrical, and results to the following expression:

$$E_{\text{SC}}^{0\to 1} = \frac{V_{\text{DD}}\tau}{2}(x_{\text{sat}\,n} - x_2) \times \left[(x_{\text{sat}\,n} + x_2 - 2x_1)S' - \frac{2C_{\text{gs}\,n}V_{\text{DD}}}{\tau}\right] + \frac{V_{\text{DD}}k_{\text{sn}}\tau}{(\alpha_n+1)}\left[(1-n-x_{\text{sat}\,n})^{\alpha_n+1} - (1-n-x_3)^{\alpha_n+1}\right] - C_{\text{gsn}}V_{\text{DD}}^2(x_3 - x_{\text{sat}\,n}) \quad (11)$$

where τ is now the transition time of the falling input, S' is the slope of the PMOS transistor current, and x_1, x_2, x_3 are related to the current pulse of the PMOS transistor. Finally, the short-circuit power dissipation P_{SC} is given by $P_{\text{SC}} = (E_{\text{SC}}^{1\to 0} + E_{\text{SC}}^{0\to 1})\mathtt{f}$, where $\mathtt{f}$ is the switching frequency.

III. Extension to Multiple-Input CMOS Gates

In order to extend the proposed energy dissipation model of the inverter to multiple-input static CMOS gates, the series-connected transistors when operate as charging or discharging block of a gate, must be reduced to an equivalent transistor. Also, a reduction technique for the case where the series-connected transistors operate as short-circuiting block, is required. The

channel width of the equivalent transistor in the case of parallel-connected transistors is simply extracted by adding the widths of the switching transistors. In the reduction techniques the effect of the internal nodes' capacitances must also be taken into account.

In our previous work [22], a reduction technique for series-connected transistors when operate as the charging or discharging block of a CMOS gate, was presented. A part of it is required for the evaluation of the short-circuit energy dissipation, and is presented here. Since, the main goal of the reduction process is the determination of the equivalent transistor's width, the following alternative current expressions of the α-power MOS model [9] are used, which include as a parameter the transistor's channel width (W)

$$I_D = \begin{cases} P_C(W/L)(V_{\rm GS} - V_{\rm TH})^{\alpha}, \\ \quad V_{\rm DS} \geq V'_{\rm DO}, \text{ Saturation region} \\ P_L(W/L)(V_{\rm GS} - V_{\rm TH})^{\alpha/2} V_{\rm DS}, \\ \quad V_{\rm DS} < V'_{\rm DO}, \text{ Linear region} \end{cases} \tag{12}$$

where $V'_{\rm DO} = P_V(V_{\rm GS} - V_{\rm TH})^{\alpha/2}$ is the drain saturation voltage, and $P_L = P_C/P_V.P_C$ and P_V are easily extracted from the current–voltage $(I$–$V)$ characteristics of the device. For the determination of the device threshold voltage $(V_{\rm TH})$ a linear approximation of the body effect is used [10], which results to the following simple formula

$$V_{\rm TH} = V_{\rm TO} + \gamma_1 V_{\rm SB} \tag{13}$$

where $V_{\rm TO}$ is the zero-bias threshold voltage, $V_{\rm SB}$ is the source-bulk voltage, and γ_1 is the body effect coefficient.

In Fig. 5, a multiple-input NAND gate is illustrated. First, the case when all transistors are switching together is analyzed. The input voltages are assumed to be ramps with input rise time τ. When the serial array performs the discharge operation, initially the topmost transistor operates in the saturation region, while the rest operate in the linear region. As shown in Fig. 6, in the case when the topmost transistor is still saturated after the end of the input transition (fast input transitions compared to the output one), its source node (2) is charged up to a plateau voltage and maintains that voltage level until all transistors enter in the linear region ($t = t_{{\rm sat}\,n1}$—Fig. 6). Then it follows the output voltage of the gate to ground. The plateau voltage (V_P) is calculated by equating the saturation current of the topmost transistor with the linear current of the rest transistors [22]. The voltage at node 2 is considered linear for the interval between the time $t_{\rm ON}$ and τ. $t_{\rm ON}$ is the time where the chain of the serial transistors starts conducting. It is calculated by analyzing the influence of the internal nodes' capacitances (gate-drain, gate-source, and diffusion capacitances) on the chain operation [22], [25]. After the calculation of the plateau voltage and the time point $t_{\rm ON}$ the slope of the voltage waveform at node 2 (V_2) can be determined. The discharge current through the serial array when the topmost transistor operates in the saturation region, is given by

$$I_D = P_C(W_1/L)[V_{\rm in} - V_{\rm TO} - (1+\gamma_1)V_2]^{\alpha_1}$$
$$I_D = P_C(W_1/L)\left[1 - \frac{(1+\gamma_1)V_2}{V_{\rm in} - V_{\rm TO}}\right]^{\alpha_1}(V_{\rm in} - V_{\rm TO})^{\alpha_1}. \tag{14}$$

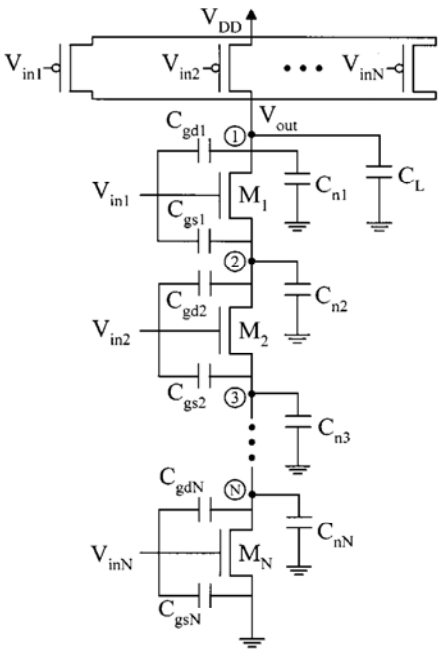

Fig. 5. Multiple-input static CMOS gate.

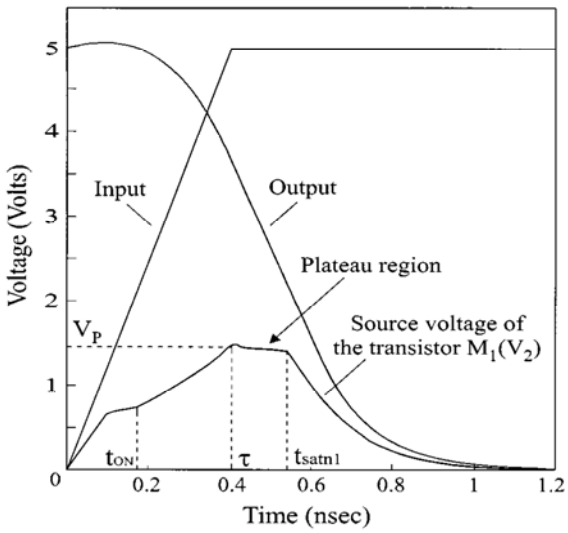

Fig. 6. Voltage waveforms of a three-input NAND gate for fast inputs.

The above equation has the same form as the current equation in the saturation region of a single transistor, the equivalent width of which is given by

$$W_{\rm eq} = W_1\left[1 - \frac{(1+\gamma_1)V_2}{V_{\rm in} - V_{\rm TO}}\right]^{\alpha_1}. \tag{15}$$

In (15), the equivalent transistor' width is given as a function of time because V_2 and $V_{\rm in}$ are linear functions of time. A reasonable approximation for the mean value of the equivalent width in the interval $[t_{\rm ON}, \tau]$ is obtained for $t = (t_{\rm ON} + \tau)/2$. This value of the equivalent width is enough for the determination of the equivalent inverter output waveform in the interval where the equivalent short-circuiting transistor operates in the linear region, which is required for the computation of the short-circuit power dissipation. In the plateau region, the equivalent width is calculated by (15) for $V_{\rm in} = V_{\rm DD}$ and $V_2 = V_P$. In [22], the

reduction process is given for the rest of the output node discharge.

In the case where the topmost transistor is entering the linear region before the end of the input transition (slow input transitions), its source node exhibits a peak value lower than the plateau one, before the input reaches its final value (Fig. 7). This peak value occurs when the topmost transistor is entering the linear region. The equivalent transistor's width is determined by using a procedure similar with that used in the previous case [22].

The output response of a multiple-input gate is a function of the number and the position of the switching transistors in the chain. When the input transition is sufficiently faster than the output one, the topmost terminal switching exhibit faster discharge operation. This is because the lower transistors must discharge the upper transistors' internal capacitances. As the input transition becomes slower, the lower terminal switching exhibits faster operation. This is because the transistor nearest to the ground has a smaller threshold voltage, while the magnitude of its gate-source voltage is greater than the other transistors in the chain. Hence, it will have a higher conductance than the other switching transistors and the discharge operation will become faster. This influence of this phenomenon is not significant in the first case where the input transition is sufficiently faster than the output one, because the input reaches its final value early (when the difference between the output voltage and the supply voltage is small).

Extensive SPICE simulations [21], [22] show that the output waveforms for different combinations of switching inputs are translational, i.e., the shape of the curve is preserved except that its transition edge is shifted to the right or to the left depending on the combination of input signals. On the basis of this observation the equivalent transistor's width for each combination of switching inputs can be determined by multiplying the one of the worst case (all inputs switching together) with a single empirical factor m. m depends on the position and number of the switching transistors, and on the relation between the input and output waveforms. As a good metric of this relation, the single lumped parameter $G = (I_{\rm DON}\tau)/(V_{\rm DD}C_L)$ is used. $I_{\rm DO}$ is the drain current at $V_{\rm GS} = V_{\rm DS} = V_{\rm DD}$ of a transistor with channel width equal to W/N (W: channel width of one transistor, N: number of series-connected transistors). Simulation results show that the factor m changes exponentially with respect to G. This enables us to use the following equation for the determination of the factor m:

$$m = m_{vf} + (m_{vs} - m_{vf})\left[1 - e^{-d(G-0.2)}\right] \qquad (16)$$

where

m_{vf} is the weight factor for very fast inputs,

m_{vs} is the weight factor for very slow inputs, and

d is a constant.

m_{vf} and m_{vs} are given by a look-up table (part of which is given in Table I). The values of the look-up table are extracted form SPICE simulations by adjusting the transistor width of an inverter to give the same output waveform with the multiple-input gate, for all the combinations of switching inputs. The values of

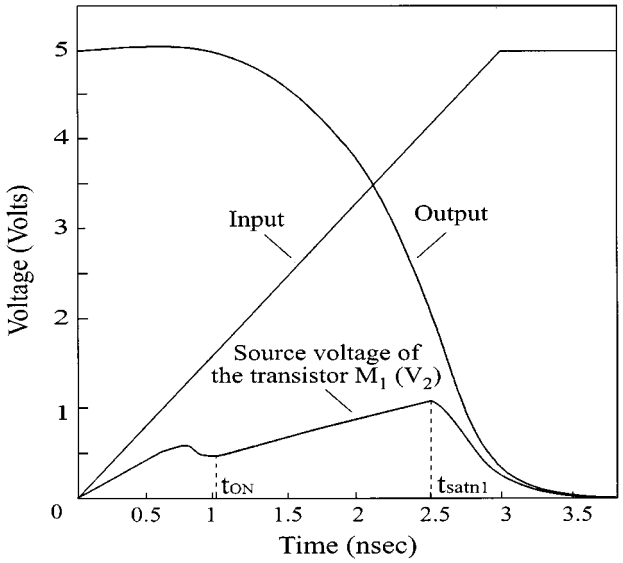

Fig. 7. Voltage waveforms of a three-input NAND gate for slow inputs.

TABLE I
VALUES OF THE FACTORS m_{vf} AND m_{vs}
(INPUT 1 CORRESPONDS TO THE TOPMOST TRANSISTOR OF THE CHAIN)

Switching Inputs	m_{vf}		m_{vs}	
	N = 3	N = 2	N = 3	N = 2
1	1.12	1.07	1.41	1.29
2	1.06	1.02	1.65	1.60
1, 2	1.03	1	1.12	1
3	1.03		2.07	
1, 3	1.09		1.15	
2, 3	1.02		1.29	
1, 2, 3	1		1	

Table I were obtained using a 0.8-μm technology, for $G = 0.2$ (very fast inputs) and $G = 10$ (very slow inputs). However, for other submicrometer technologies these values are almost the same, because they mainly depend on the number and position of the switching inputs. The constant d is equal to 0.42 for the used technology. This value is almost independent of N, at least for $2 \leq N \leq 5$. In Fig. 8, a comparison between the values of factor m derived from the exponential function (16) with those produced from SPICE simulations is illustrated, for a three-input NAND gate. The above reduction technique of series-connected transistors when they operate as charging or discharging block in a CMOS gate, results in output voltage waveforms that are very close to those derived from SPICE simulations (as shown in [22]).

In the following, a reduction technique for series-connected transistors when operate as the short-circuiting block of a static CMOS gate, is presented. The short-circuiting block has a secondary influence compared to that of the charging or discharging block. However, this influence becomes significant in the case of slow input transitions [24].

Consider the multiple-input NAND gate of Fig. 5, with a rising output voltage waveform. The equivalent transistor's width is calculated by

$$W_{\rm eq} = qW_L \tag{17}$$

where

$$\frac{1}{W_L} = \frac{1}{W_1} + \frac{1}{W_2} + \cdots + \frac{1}{W_N}$$

and q is a correction factor which depends on the number of switching transistors in the chain. The values of factor q are extracted from SPICE simulations by excluding the internal nodes' capacitances of the chain (the parameters $T_{\rm OX}, C_{\rm GDO}, C_{\rm GSO}$, and the dimensions of the diffusions areas are set to zero), and adjusting the transistor width of an inverter to give the same output with the multiple-input gate, for all the combinations of switching inputs. We observe that for zero internal nodes' capacitances, the output response of the gate is independent from the position of the switching transistors, and depends only on the number of the switching transistors. This is mainly due to the fact that the source voltages of the switching transistors in the chain are very small compared to the source voltages when the serial chain carries both the load and the short-circuit current. Thus, the influence of body effect in this case is negligible. When the number of the switching transistors is increased the value of factor q is decreased. This is due to the lower conductance of the switching transistors than those that are already ON. In Table II, the values of factor q are given for a 0.8-μm technology process. The value $q = 1$ correspond to the traditional model for the reduction of series-connected transistors. It is quite accurate when all transistors operate in the linear region. However, even in the case when all transistors are switching the value of q is higher than "1," due to the fact that the topmost transistor is saturated after its linear region.

The second step of the reduction process is to include the influence of the internal nodes' capacitances of the transistors that are already ON. The charging operation is slower when the switching transistors are close to ground, because the capacitances of the ON transistors must be charged together with the output capacitance of the gate. In order to model the effect of the ON transistors' capacitances, the capacitance C_O is added to the output capacitance (C_L)

$$C_O = \left[\sum_{i=1}^{k} r_i C_i\right] - r_k C_{gdk} \tag{18}$$

where

$$C_i = C_{gdi} + C_{gsi-1} + C_{ni} \quad \text{and} \quad r_i = \frac{N+1-i}{N}.$$

k is the drain node of the first switching transistor [counting from the output node to ground (Fig. 5)]. The coefficient r_i is inserted because the charge variation due to each capacitance occurs through a different number of channels. Thus, the contribution of the internal nodes' capacitances depends on their relative position in the chain. The gate-drain and gate-source capacitances of the ON transistors are given by [23]

$$C_{gdi} = C_{gsi} = \tfrac{1}{2} C_{\rm ox} W_i L_i + C_{gd(s)o} W_i \tag{19}$$

due to the fact that the ON transistors operate in the linear region in most time of output transition. The capacitance C_{gdk} is excluded because it is taken into account in the feedforward effect of the gate, which is modeled below.

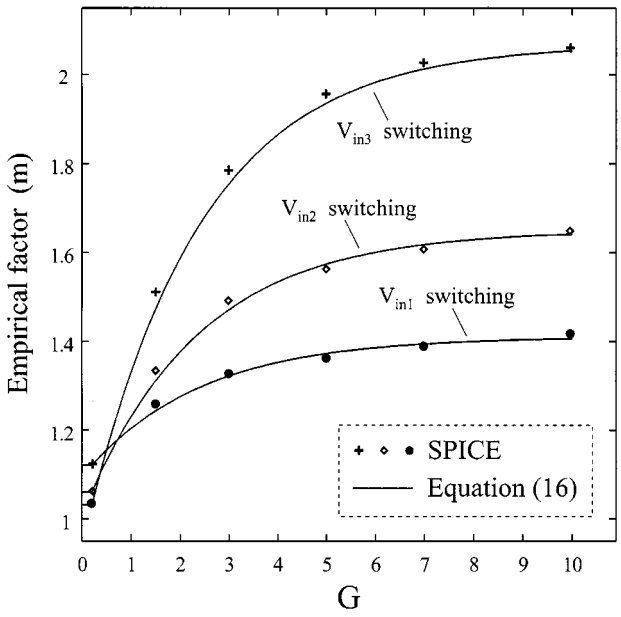

Fig. 8. Empirical factor m as a function of $G = (I_{\rm DON}\tau)/(V_{\rm DD}C_L)$ for a three-input NAND gate.

TABLE II
VALUES OF THE CORRECTION FACTOR q

No. of switching transistors	q		
	N = 4	N = 3	N = 2
1	1.90	1.72	1.58
2	1.45	1.31	1.11
3	1.15	1.08	
4	1.05		

As shown in Fig. 9, the contributions of the gate-drain and gate-source capacitances of series-connected transistors (when they operate as short-circuiting block) to the equivalent input-to-output capacitance of a gate, are accounted for by capacitances between the switching inputs and the output (C_{M1}, C_{M2}, C_{M3}). Note, that the contribution of nonswitching transistors is zero. The undershoot which is caused to the early part of the rising output waveform is due to the feedforward effect (i.e., the charge through the switching transistors' gate-source and gate-drain capacitances). This charge is transferred through a different number of channels, depending on the relative position of each switching transistor in the chain. Therefore, the contribution of each switching transistor to the equivalent input-to-output capacitance is modeled as

$$C_{Mk} = r_k C_{gdk} + r_{k+1} C_{gsk} \tag{20}$$

where $r_k = (N + 1 - k)/N$, and k is the drain node of the switching transistor M_k. When more than one inputs are switching together, the equivalent input-to-output capacitance can be found by adding the C_{Mk}s of the corresponding single switching cases.

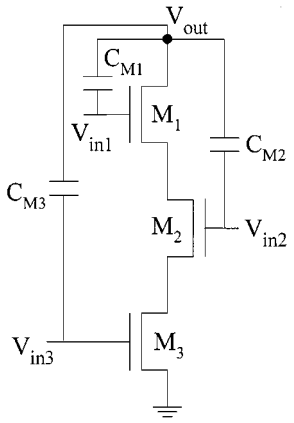

Fig. 9. Contribution of series-connected transistors (when they operate as short-circuiting block) to the gate equivalent input-to-output coupling capacitance.

As shown in Table III, the results derived from (20) are very close to those produced from SPICE simulations. The contribution of a switching transistor in the equivalent input-to-output capacitance can be measured using SPICE by adjusting an input-to-output capacitance in an inverter so that the undershoot of the inverter rising output waveform to be the same with the undershoot of the gate output waveform.

The contributions of the gate-drain and gate-source capacitances of series-connected transistors to the gate-source capacitance of the equivalent short-circuiting transistor, which is required for the evaluation of the short-circuit energy dissipation, is modeled in a similar way by capacitances between the switching inputs and the ground (or between the switching inputs and the power supply in case of PMOS transistors). They are calculated by (20) if we substitute r_k and r_{k+1} with $(1-r_k)$ and $(1-r_{k+1})$, respectively.

The channel width of the equivalent transistor in the case of parallel-connected transistors is extracted by adding the channel widths of the switching transistors. The diffusion capacitances of all parallel-connected transistors and the gate-drain capacitances (overlap) of the OFF transistors are added to the equivalent output capacitance of the gate. The gate-drain capacitances of the switching parallel-connected transistors are added to the equivalent input-to-output capacitance of the gate. Finally, the sum of gate-source capacitances of the switching transistors gives the equivalent short-circuiting transistor's gate-source capacitance, which is required for the calculation of the gate short-circuit energy dissipation.

In the case of overlapping inputs, the existing waveform representation techniques for series—[20], [25] and parallel-connected [20], [26] transistors can be used, which reduce the overlapping input signals of a multiple-input CMOS gate to a single effective signal. When this signal is applied to all gate inputs, the gate will have the same output response with that of the actual (overlapping) inputs.

IV. Model Validations and Discussion

In this section, we illustrate the accuracy of the proposed short-circuit energy dissipation model for static CMOS structures. In Fig. 10, the inverter short-circuit energy dissipation during one switching cycle (both falling and rising output transitions) is plotted as a function of the input transition time. A commercial CMOS process technology of 0.8 μm with a supply voltage of 5 V and an output load equal to 0.2 pF have been used to verify the accuracy of the proposed model. The transistors' model parameters and dimensions are listed in Table IV. In order to achieve symmetrical inverter, the widths of the transistors have been selected so as the drain currents at $V_{\rm GS} = V_{\rm DS} = V_{\rm DD}$ be equal. The basic level-3 parameters of the SPICE model are listed in Table V. Results using the approaches for the evaluation of the short-circuit energy dissipation presented in [4], [5], [9], [11], and [13] are also given. It can be observed that our model gives results closer to those derived from SPICE simulations than the other methods. The error in most cases is less than 15%. This occurs because the model includes the influences of the short-circuit current and the gate-to-drain coupling capacitance on the inverter output waveform. Moreover, the effect of the short-circuiting transistor's gate-source capacitance is taken into account.

The formula presented in [9] gives consistently larger results than SPICE, because it is based on the assumption of zero-load capacitance. The methods presented in [4], [5], and [11] overestimate the short-circuit energy because they do not include the effects noted above. The error becomes large when the input transition time is large and the capacitive load is small. Moreover, the method used in [4], [5] is based on the square-law MOS model, which does not reproduce the current characteristics of short-channel devices well, while in [11] an evaluation of gamma function is required, which is too computational expensive and leads to large energy values for slow input transitions. In [13], the inverter output is approximated by a linear waveform. This results in significant relative error for fast input transitions. Also, in [13], some additional simplifications are used, in order to determine the time point where the short-circuiting transistor changes from the linear to the saturation region, and the ending point of the output voltage overshoot, while in our model the calculation accuracy of these time points is high (error less than 0.5% in most cases).

In [8], the derived average short-circuit current depends on the ratio between the output and the input transition times of the inverter. However, in the cases where this ratio is lower than 3, the average current may exceed the maximum average short-circuit current obtained for zero-load capacitance [2], [9]. For example, in an inverter with equal input and output transition times, the short-circuit energy dissipation in one switching cycle which is evaluated using the formula of [8] is more than twice the energy calculated using the formula of [9].

Fig. 11(a) shows a comparison between the calculated and the simulated inverter short-circuit energy dissipation during one switching cycle as functions of input transition time, and for two different values of capacitive load (0.1 and 0.2 pF). An important issue is to study the contribution of the short-circuit energy dissipation to the total energy dissipation (capacitive plus short-circuit). In Fig. 11(b), the short-circuit energy dissipation percentage of the total energy dissipation during one switching cycle is plotted as a function of the input transition time for two values of output load. The results show that the contribution of the short-circuit energy to the total energy dissipation increases

TABLE III
CONTRIBUTION OF EACH SWITCHING TRANSISTOR TO THE EQUIVALENT INPUT-TO-OUTPUT CAPACITANCE ($W_n = 12\ \mu$m, $L_n = 0.8\ \mu$m, $C_{ox} = 2.18$ fF/μm^2, $C_{gso} = C_{gdo} = 0.35$ fF/μm)

Switching Input	C_{Mk} (fF)					
	N = 4		N = 3		N = 2	
	Eq. (20)	SPICE	Eq. (20)	SPICE	Eq. (20)	SPICE
1	25.4	25.5	24.6	24	22.2	23
2	18.5	18	14.8	14.5	7.4	8.6
3	11	10	4.9	5.3		
4	3.7	3.5				

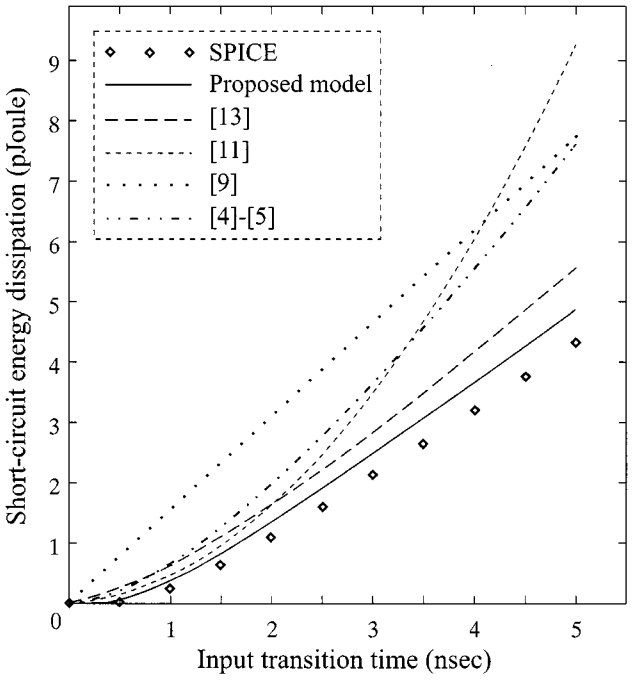

Fig. 10. Inverter short-circuit energy dissipation during one switching cycle, as a function of input transition time.

when the input transition time is increased and/or the capacitive load is reduced. Hence, the percentage of the short-circuit energy dissipation increases when the input signal is slow compared to the output one. As it can be observed, for sufficiently slow inputs the short-circuit energy dissipation may exceed 40% of the total energy dissipation. This fact indicates the need for accurate and efficient models in estimating the short-circuit energy dissipation.

Fig. 12 shows a comparison between the calculated and the simulated inverter short-circuit energy dissipation during one switching cycle as functions of input transition time, and for two different values of supply voltage (2.5 and 5 V). A capacitive load of 0.2 pF has been used for the measurements and the calculations. It can be observed that the proposed short-circuit energy model is also valid for low supply voltages. An important point to note, is that if the supply voltage is lowered to be below the sum of the threshold voltages of the transistors ($V_{THn}+V_{THp}$),

TABLE IV
MOSFET MODEL PARAMETERS USED IN CALCULATIONS

Parameter	NMOS	PMOS
L (μm)	0.8	0.8
W (μm)	4	6.55
I_{D0} (mA)	1.72	1.72
$\lvert V_{D0}\rvert$ (V)	1.30	2.45
α	1.245	1.37
$\lvert V_{TH}\rvert$ (V)	0.844	0.734
C_{ox} (fF/μm^2)	2.18	2.18
C_{gdo}, C_{gso} (fF/μm)	0.35	0.35

the short-circuit current can be virtually (since subthreshold currents will still flow [1]) eliminated, because both devices cannot conduct simultaneously for any value of the input voltage.

In Figs. 13 and 14, the short-circuit energy dissipation during one switching cycle for three- and four-input NAND gates, is plotted as a function of the input transition time, for different cases of switching inputs. The characteristics of the gates used are: $L_n = L_p = 0.8\ \mu$m, $W_n = 8\ \mu$m, $W_p = 4\ \mu$m, $C_L = 0.15$ pF, and $V_{DD} = 5$ V. The curves with the solid and dashed lines have been produced from the proposed analytical model after the application of the reduction techniques presented in Section III. The curves with the symbols have been produced from SPICE simulations. The relative error is maintained at the same level with that of the inverter.

In the case of fast inputs, the lowest short-circuit energy is dissipated when all transistors are switching together. The major reason is that in this case the equivalent input-to-output coupling capacitance and the gate-source capacitance of the equivalent short-circuiting transistor are larger than those of the other two cases (top or bottom transistor is switching). Also, the short-circuit energy in the case where the bottom transistor is switching, is lower than that of the case where the top transistor is switching. This occurs because the charge and the discharge operation of the output is faster in the second case.

For slow inputs, the short-circuit energy dissipation is greater when all transistors are switching together. This occurs mainly

TABLE V
BASIC SPICE LEVEL-3 PARAMETERS USED IN SIMULATIONS

Parameter	NMOS	PMOS
Transconductance parameter - K_P (A/V^2)	1.03×10^{-4}	3.565×10^{-5}
Gate oxide thickness - T_{OX} (m)	15.5×10^{-9}	15.5×10^{-9}
Maximum drift velocity of carries – V_{MAX} (m/sec)	6.19×10^{4}	6.13×10^{4}
Zero-bias threshold voltage – V_{TO} (V)	0.844	-0.734
Surface inversion potential – PHI (V)	0.791	0.757
Body effect parameter – GAMMA ($V^{1/2}$)	0.653	0.468
Surface mobility - U_O ($cm^2/V.sec$)	462	160
Substrate doping – N_{SUB} (cm^{-3})	63.8×10^{15}	32.8×10^{15}
Gate-drain overlap capacitance – C_{GDO} (F/m)	3.5×10^{-10}	3.5×10^{-10}
Gate-source overlap capacitance – C_{GSO} (F/m)	3.5×10^{-10}	3.5×10^{-10}
Gate-bulk overlap capacitance – C_{GBO} (F/m)	1.5×10^{-10}	1.5×10^{-10}
Zero-bias junction capacitance – C_J (F/m^2)	0.29×10^{-3}	0.49×10^{-3}
Zero-bias perimeter capacitance – C_{JSW} (F/m)	0.23×10^{-9}	0.21×10^{-9}
Bulk-junction grading coefficient – M_J	0.46	0.47
Perimeter capacitance grading coefficient - M_{JSW}	0.33	0.29
Bulk-junction potential – PB (V)	0.86	0.8
Metallurgical junction depth – X_J (m)	0.08×10^{-6}	0.087×10^{-6}
Width effect on threshold voltage – DELTA	0.237	0.949

because in the case of falling output the equivalent short-circuiting transistor (which becomes from the reduction of three or four parallel-connected transistors) exhibits larger width than that of the other two cases. However, the discharge operation is faster and the coupling capacitances are larger. These two effects tend to compensate for the first one when the number of switching inputs is increased (Fig. 14). The short-circuit energy in the case where the bottom transistor is switching, is greater than that of the case where the top transistor is switching. This is mainly due to the faster discharge operation of the first case.

Comparing the results of Figs. 13 and 14, we observe that as the number of transistors is increased in static CMOS gates, the short-circuit energy dissipation is decreased. This is due to the fact that the falling output transitions become slower, and the coupling capacitance are larger (in the case where all inputs are switching).

The SPICE simulation results used in the previous validations (Figs. 10–14), have been obtained by using the subcircuit proposed by Kang [27]. Fig. 15 shows the scheme that is used in order to measure the short-circuit energy dissipation during the falling output transition of a static CMOS structure. First, we perform a measurement for an extremely small input transition time and a typical output capacitance. With this measurement the energy of the currents through the coupling capacitances ($I_{C_{\rm gsp-eq}}, I_{C_{M-\rm eq}}$), and the internal gate capacitances ($I_{\rm int}$), is determined. This energy is almost independent of the input transition time and the output capacitance, because all voltages before and after the switching event are identical (i.e., the charge on these capacitances is almost constant). On the contrary, as mentioned in Section II, the short-circuit energy dissipation for very fast input transitions is zero. In the following, a second measurement is performed for the desired input transition time and output capacitance. Then, the short-circuit energy dissipation of the structure is evaluated by subtracting the result of the first measurement from the result of the second measurement. The short-circuit energy dissipation during the rising output transition of the structure is measured in a similar way, by using a measurement subcircuit connected between the NMOS block and the ground.

As minimum feature sizes for CMOS circuits scale downward, the influence of the resistive component of the interconnect load on the circuit behavior, is increased. Hence, some short-circuit energy dissipation models [28], [29] have been proposed in order to handle CMOS gates driving resistance–capacitance (RC) load. However, our analytical model that uses purely capacitive load can be interfaced with a methodology considering the effect of RC interconnect load, by using the "effective load capacitance—$C_{\rm eff}$" [30]. In this, an analytical expression

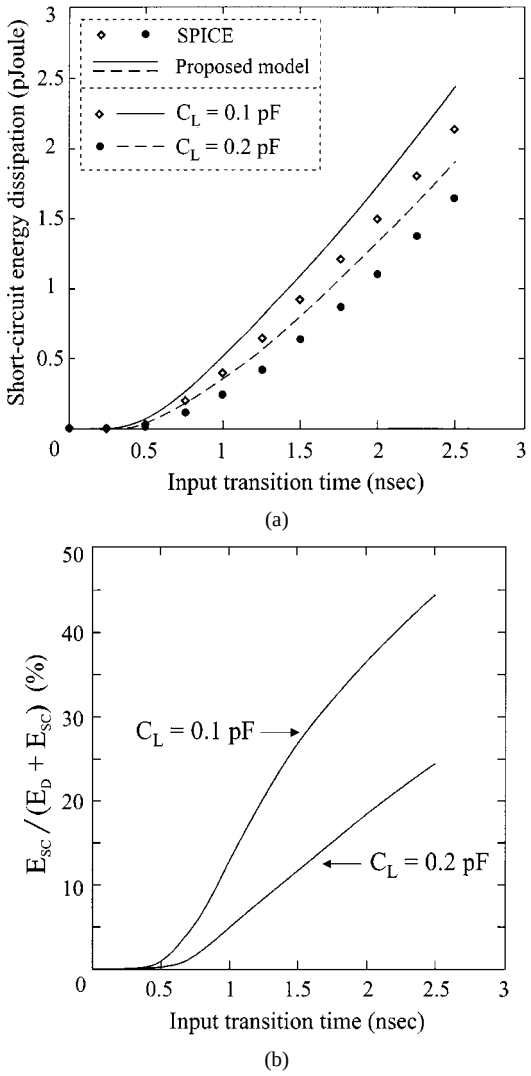

Fig. 11. Inverter short-circuit energy dissipation (a) and contribution of the short-circuit energy to the total energy dissipation (b) during one switching cycle, for two values of output load ($C_L = 0.2$ pF, $C_L = 0.1$ pF).

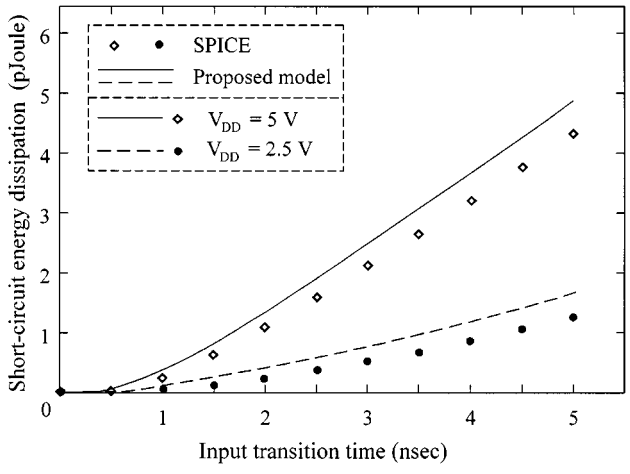

Fig. 12. Inverter short-circuit energy dissipation during one switching cycle, for two values of supply voltage ($V_{DD} = 2.5$ V, $V_{DD} = 5$ V).

for C_{eff} is derived for any RC load. The approach gives accurate gate output waveforms, especially for the part of the output transition in which short-circuit energy is dissipated [30].

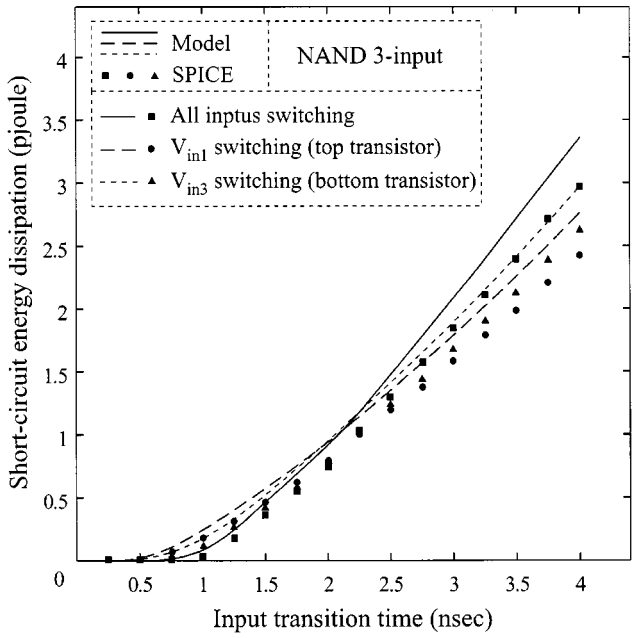

Fig. 13. Short-circuit energy dissipation of a three-input NAND gate during one switching cycle, as a function of input transition time.

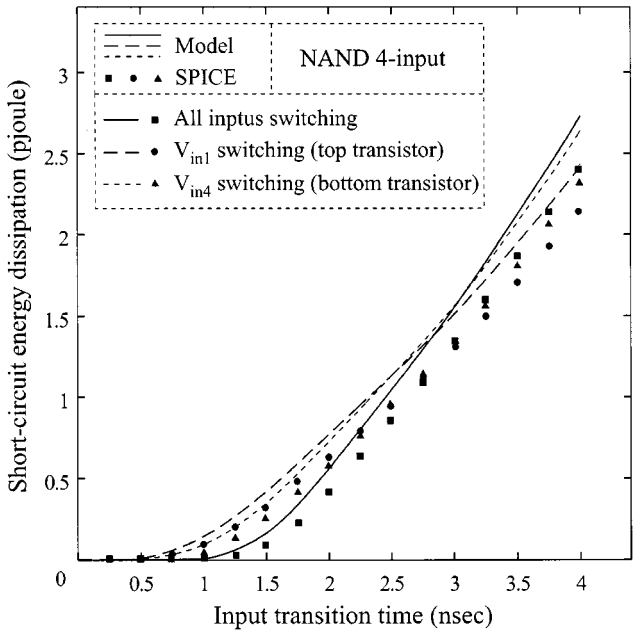

Fig. 14. Short-circuit energy dissipation of a four-input NAND gate during one switching cycle, as a function of input transition time.

V. Conclusion

An analytical model for the short-circuit energy dissipation of submicrometer CMOS structures, on the basis of a CMOS inverter, has been presented. It takes into account the influences of both transistor currents and the gate-to-drain coupling capacitance on the inverter output wavefrom. Also, the effect of the short-circuiting transistor's gate-source capacitance has been included. Validations have been performed for different input transition times and output loads. The results produced by the model show very good agreement with SPICE simulations and greater accuracy than those of previous works. The inverter

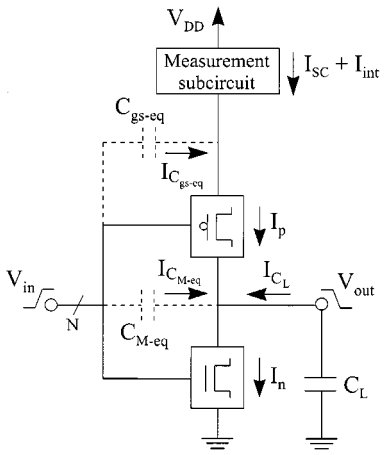

Fig. 15. Measurement of short-circuit energy dissipation in CMOS structures for a falling output waveform.

model has been extended to CMOS multiple-input gates using reduction techniques of series- and parallel-connected transistors.

REFERENCES

[1] A. P. Chandrakasan and R. W. Brodersen, *Low-Power Digital CMOS Design.* Norwell, MA: Kluwer Academic, 1995, pp. 55–104.

[2] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 468–473, Aug. 1984.

[3] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 285–289, Sept. 1968.

[4] N. Hedenstierna and K. O. Jeppson, "CMOS circuit speed and buffer optimization," *IEEE Trans. Computer-Aided Design*, vol. CAD-6, pp. 270–281, Mar. 1987.

[5] ——, "Comments on 'A module generator for optimized CMOS buffers'," *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 180–181, Jan. 1993.

[6] Q. Wang and S. B. K. Vrudhula, "On short circuit power estimation of CMOS inverters," in *Proc. IEEE Int. Conf. Computer Design*, Oct. 1998, pp. 62–67.

[7] L. Bisdounis, S. Nikolaidis, and O. Koufopavlou, "Propagation delay and short-circuit power dissipation modeling of the CMOS inverter," *IEEE Trans. Circuits Syst. I*, vol. 45, pp. 259–270, Mar. 1998.

[8] S. Turgis, N. Azemard, and D. Auvergne, "Explicit evaluation of short-circuit power dissipation for CMOS logic structures," in *Proc. Int. Symp. Low-Power Design*, Apr. 1995, pp. 129–134.

[9] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, pp. 584–594, Apr. 1990.

[10] ——, "A simple MOSFET model for circuit analysis," *IEEE Trans. Electron Dev.*, vol. 38, pp. 887–894, Apr. 1991.

[11] S. R. Vemuru and N. Scheinberg, "Short-circuit power dissipation estimation for CMOS logic gates," *IEEE Trans. Circuits Syst. I*, vol. 41, pp. 762–765, Nov. 1994.

[12] A. Hirata, H. Onodera, and K. Tamaru, "Estimation of short-circuit power dissipation for static CMOS gates," in *IEICE Trans. Fundament. Electron., Commun. Comput. Sci.*, vol. E79-A, Mar. 1996, pp. 304–311.

[13] S. Turgis and D. Auvergne, "A novel macromodel for power estimation in CMOS structures," *IEEE Trans. Comput.-Aided Design*, vol. 17, pp. 1090–1098, Nov. 1998.

[14] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1988, pp. 175–181.

[15] D. Auvergne, private communication, Nov. 1998.

[16] J. M. Daga, S. Turgis, and D. Auvergne, "Design oriented standard cell delay modeling," in *Proc. Int. Wkshp. Power Timing Modeling, Optimiz. Simulat.*, Sept. 1996, pp. 265–274.

[17] J. M. Daga and D. Auvergne, "A comprehensive delay macro modeling for submicrometer CMOS logics," *IEEE J. Solid-State Circuits*, vol. 34, pp. 42–55, Jan. 1999.

[18] L. Bisdounis, O. Koufopavlou, and S. Nikolaidis, "Accurate evaluation of the CMOS short-circuit power dissipation for short-channel devices," in *Proc. IEEE Int. Symp. Low-Power Electron. Design*, Aug. 1996, pp. 189–192.

[19] D. Liu and C. Svensson, "Power consumption estimation in CMOS VLSI chips," *IEEE J. Solid-State Circuits*, vol. 29, pp. 663–670, June 1994.

[20] A. Nabavi-Lishi and N. C. Rumin, "Inverter models of CMOS gates for supply current and delay evaluation," *IEEE Trans. Comput.-Aided Design*, vol. 13, pp. 1271–1279, Oct. 1994.

[21] J. T. Kong and D. Overhauser, *Digital Timing Macromodeling for VLSI Design Verification.* Norwell, MA: Kluwer Academic, 1995, pp. 125–169.

[22] L. Bisdounis and O. Koufopavlou, "Modeling the dynamic behavior of series-connected MOSFET's for delay analysis of multiple-input CMOS gates," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 6, June 1998, pp. 342–345.

[23] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*. New York: McGraw-Hill, 1993, pp. 183–191.

[24] L. Bisdounis, S. Nikolaidis, and O. Koufopavlou, "Analytical transient response and propagation delay evaluation of the CMOS inverter for short-channel devices," *IEEE J. Solid-State Circuits*, vol. 33, pp. 302–306, Feb. 1998.

[25] A. Chatzigeorgiou and S. Nikolaidis, "Collapsing the transistor chain to an effective single equivalent transistor," in *Proc. IEEE Design, Automa. Test Eur.*, Feb. 1998, pp. 2–6.

[26] Y. H. Jun, K. Jun, and S. B. Park, "An accurate and efficient delay time modeling for MOS logic circuits using polynomial approximation," *IEEE Trans. Comput.-Aided Design*, vol. 8, pp. 1027–1032, Sept. 1989.

[27] S. M. Kang, "Accurate simulation of power dissipation in VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 889–891, Oct. 1986.

[28] A. Hirata, H. Onodera, and K. Tamaru, "Analytical formulas of output waveform and short-circuit power dissipation for static CMOS gates driving a CRC π load," in *IEICE Trans. Fundament. Electron., Commun. Comput. Sci.*, vol. E81-A, Mar. 1998, pp. 462–469.

[29] V. Alder and E. G. Friedman, "Delay and power expressions for a CMOS inverter driving a resistive-capacitive load," *Analog Integrat. Circuits Signal Processing J.*, vol. 14, pp. 29–39, Jan. 1997.

[30] J. Qian, S. Pullela, and L. Pillage, "Modeling the 'effective capacitance' for the RC interconnect of CMOS gates," *IEEE Trans. Comput.-Aided Design*, vol. 13, pp. 1526–1535, Dec. 1994.

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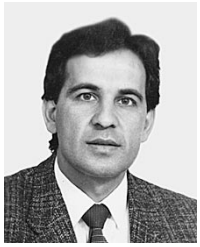

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