Analytical Model for the CMOS Short-Circuit Power Dissipation

L. BISDOUNIS,[a] S. NIKOLAIDIS,[b] O. KOUFOPAVLOU[a]

[a] *VLSI Design Laboratory, Department of Electrical & Computer Engineering, University of Patras, 26500 Patras, Greece*
[b] *Electronics & Computers Division, Department of Physics, Aristotle University of Thessaloniki, 54006 Thessaloniki, Greece*

ABSTRACT: A significant part of the power dissipation in CMOS digital circuits is due to the short-circuit currents. In this paper an accurate analytical model for the evaluation of the CMOS short-circuit power dissipation, on the basis of a CMOS inverter, is presented. The innovation of the proposed approach against previous works is due to the accurate, analytical expressions of the inverter output waveform which include for the first time the effects of both transistor currents and the gate-to-drain coupling capacitance. The α-power law MOS model which considers the carriers' velocity saturation effects of short-channel devices is used. The results produced by the suggested model show very good agreement with SPICE simulations.

INTRODUCTION

Recently, the desirability of portable operation of many electronic systems, demands high speed computations combined with low power dissipation, has become clear (Chandrakasan et al., 1992). Since power dissipation is one of the most critical parameters in VLSI circuits, accurate and efficient power evaluation during the design phase is required in order to meet the power specifications without a costly redesign process. Much effort has to be devoted for the extraction of power dissipation models for basic circuits, which can be incorporated in switch and logic simulators, optimizing the design verification procedure.

Power dissipation in CMOS circuits consists mainly of two parts, the capacitive and the short-circuit power dissipation. Capacitive dissipation, caused by charging and discharging the load capacitance, is well understood and easy to be estimated. During switching in a static CMOS structure, a direct path from the power supply to the ground is established, resulting in short-circuit power dissipation.

The focus of this work is on the analytical evaluation of short-circuit power dissipation in CMOS inverters. Specifically, for the operation regions which are required for the evaluation of the short-circuit power dissipation, we derive analytical expressions of the output waveform. It is important to have an accurate model for the CMOS inverter short-circuit power dissipation, since several fast methods for reducing a CMOS gate to an equivalent inverter have been proposed (Nabavi-Lishi and Rumin, 1994; Jun et al., 1989).

Analytical expressions for the output waveform including the input slope effects was presented by Hedenstierna and Jeppson (1987) and Kayssi et al. (1992), where the influence of the short-circuit current was neglected. The results reported in these papers are based on the Shichman and Hodges (1968) square-law MOS model that ignores the carriers' velocity saturation effect. Jeppson (1994) presented expressions of the inverter output waveform considering the currents through both transistors, and the gate-to-drain capacitance, but his results were still based on the square-law MOS model.

Sakurai and Newton (1990, 1991) introduced the α-power (n-power in Sakurai and Newton (1991)) law MOS model that considers the velocity saturation effect, which becomes prominent in short-

Correspondence to: Dr. L. Bisdounis.
Integrated Computer-Aided Engineering, 5(2) 129–140 (1998)

1069-2509/98/$8.00 © 1998 IOS Press. All rights reserved

channel devices, and presented analytical expressions for the inverter output waveform. However, in Sakurai and Newton (1990) the short-circuit current is neglected, while in Sakurai and Newton (1991) a fictitious input ramp is used in order to approximate the CMOS inverter by a NMOS circuit. This approximation is exact only for extreme cases of input ramps, and does not model accurately the early part of the inverter output waveform, where short-circuit power is dissipated.

The first closed-form expression for the evaluation of the short-circuit power dissipation in a CMOS inverter was presented by Veendrick (1984) where zero load capacitance and current waveform which is mirror symmetric about a central vertical axis (at the half of the input transition time) were assumed. Also, it is considered that the transistor which is switched from cutoff to saturation remains in saturation during the entire time when short-circuit current is conducted. This expression gives the maximum value of the short-circuit power dissipation, and is based on the square-law MOS model.

More recently, in Hedenstierna and Jeppson (1987, 1992) an expression for the short-circuit energy dissipation of the CMOS inverter, without the simplifications of Veendrick (1984), was derived. However, as mentioned above the square-law MOS model was used and the expression of the output waveform was derived with negligible short-circuit current. A closed-form expression for the evaluation of the short-circuit power dissipation, based on an expression of the output waveform which considers the current through both transistors, was presented by Bisdounis et al. (1996), but was also based on the square-law MOS model.

Sakurai and Newton (1990) presented a formula for the short-circuit energy dissipation during one switching cycle which is a direct extension of the formula presented in Veendrick (1984). The only difference is the use of the α-power MOS model for the saturation current expression instead of the square-law MOS model, while all the assumptions of Veendrick (1984) are retained. In Cherkauer and Friedman (1995), a substitution of the input transition time as given by Sakurai and Newton (1990) into the formula of the short-circuit dissipation also presented by Sakurai and Newton (1990), was proposed. This results in an expression for the short-circuit dissipation including the load capacitance, which is not valid due to the initial assumption of zero load capacitance.

Vemuru and Scheinberg (1994) proposed a formula for the evaluation of the short-circuit power dissipation based on the α-power MOS model, where the analytical expression of the output waveform does not include the influences of the short-circuit current and the gate-to-drain coupling capacitance. Also, it is assumed that the load transistor operates in the saturation region during the time when short-circuit current flows. A formulation of the short-circuit power dissipation through an equivalent short-circuit capacitance is presented in Turgis et al. (1995), where mean charge conservation across the CMOS structure and a linear rough approximation of the output waveform are used. Recently, in Hirata et al. (1996), the short-circuit current waveform was approximated with a piece-wise linear function of time, in order to estimate the short-circuit energy dissipation. However, the energy of the reverse current due to the gate-to-drain coupling capacitance is subtracted from the short-circuit energy dissipation, resulting in an underestimation. This reverse current is provided from the inverter input, so its energy component cannot be included in the short-circuit energy dissipation which is due to the direct current from the power supply to the ground.

In this work, an analytical expression for the evaluation of the short-circuit power dissipation in a CMOS inverter, based on the α-power law MOS model (Sakurai and Newton, 1990) is derived. For the derivation, analytical expressions of the output waveform which consider the current through both transistors are used. In order to obtain better accuracy, avoiding an overestimation of the short-circuit power dissipation, we consider the influence of the gate-to-drain coupling capacitance. The presented expression shows the influence of the inverter design characteristics, the load capacitance and the slope of the input waveform driving the inverter on the short-circuit power dissipation.

The rest of the paper is organized as follows. In the second section, analytical expressions of the inverter output response to a rising input, for the operation regions which are required for the evaluation of the short-circuit power dissipation, are derived. Our approach for the evaluation of the short-circuit power dissipation is presented in the third section. Results, comparisons with previous works and SPICE measurements are given in the fourth section. Also in this section, the impact of the short-circuit component on the total power dissipation is discussed. Finally, we conclude in the last section.

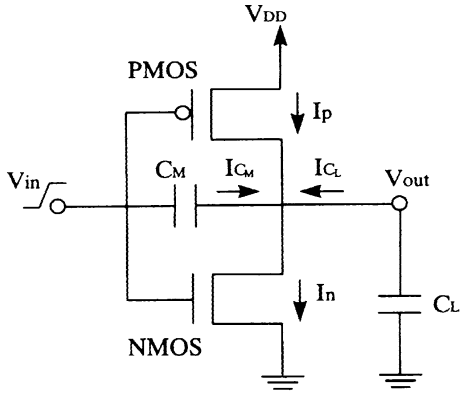


Figure 1 The CMOS inverter.

INVERTER OUTPUT WAVEFORM ANALYSIS

The inverter input voltage is assumed to be a pulse. The pulse edges are given by

$$V_{in} = \begin{cases} \dfrac{V_{DD}t}{\tau_r}, & \text{rising edge,} \\ V_{DD}\left(1 - \dfrac{t}{\tau_f}\right), & \text{falling edge,} \end{cases} \quad (1)$$

where τ_r and τ_f are the input rise and fall times, respectively. The expressions of the output waveform presented in the rest of the paper are for the rising input edge. The analysis for the falling input edge is symmetrical. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter (Figure 1), taking into account the gate-to-drain capacitive coupling (C_M), is derived from the application of the Kirchoff's current law to the output node

$$I_{C_L} + I_{C_M} + I_p - I_n = 0,$$
$$C_L \frac{dV_{out}}{dt} = C_M\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) + I_p - I_n. \quad (2)$$

The output load consists of the inverter drain junction capacitances, the gate capacitances of fanout gates and the interconnect capacitances. The equivalent gate-to-drain capacitance C_M is the sum of the gate-to-drain capacitances of both transistors

$$C_M = C_{gd-NMOS} + C_{gd-PMOS}.$$

The gate-to-drain capacitance of a transistor is the sum of the gate-to-drain overlap capacitance and a part of gate-to-channel capacitance (Weste and Eshraghian, 1993). The overlap capacitance is voltage independent and is given by

$$C_{gd-overlap} = WC_{gdo},$$

where W is the effective width of the transistor and C_{gdo} is the gate-to-drain overlap capacitance per micron. In the cutoff region of the transistor there is no conducting channel, and in the saturation region the channel does not extend to the drain. Therefore, the gate-to-drain capacitance due to the channel charge is equal to zero. In the linear region the distributed gate-to-channel capacitance may be viewed as being shared equally between the source and the drain. Thus in this case

$$C_{gd-channel} = \frac{1}{2}C_{ox}WL,$$

where C_{ox} is the gate oxide capacitance per unit area and L is the effective length of the transistor.

For the expressions of the transistor currents the four-parameter α-power law MOS model is used. The parameters are the velocity saturation index (α), the drain current (I_{D0}) at $V_{GS} = V_{DS} = V_{DD}$, the drain saturation voltage (V_{D0}) at $V_{GS} = V_{DD}$, and the threshold voltage (V_{TH}). After normalizing voltages with respect to V_{DD}, i.e. $u_{in} = V_{in}/V_{DD}$, $u_{out} = V_{out}/V_{DD}$, $n = V_{TH_n}/V_{DD}$, $p = |V_{TH_p}|/V_{DD}$, $u_{don} = V_{D0n}/V_{DD}$, $u_{dop} = V_{D0p}/V_{DD}$ and using the variable $x = t/\tau_r$, the NMOS and PMOS device currents (Sakurai and Newton, 1990) of the CMOS inverter are given by the following equations:

$$I_n = \begin{cases} 0, & \\ x \le n, & \text{Cutoff region,} \\ k_{sn}(x-n)^{\alpha_n}, & \\ u_{out} \ge u'_{don}, & \text{Saturation region,} \\ k_{ln}(x-n)^{\alpha_n/2}u_{out}, & \\ u_{out} < u'_{don}, & \text{Linear region,} \end{cases} \quad (3)$$

where $k_{sn} = \frac{I_{D0n}}{(1-n)^{\alpha_n}}$, $k_{ln} = \frac{I_{D0n}}{u_{don}(1-n)^{\alpha_n/2}}$, $u'_{don} = u_{don}\left(\frac{x-n}{1-n}\right)^{\frac{\alpha_n}{2}}$, and

$$I_p = \begin{cases} k_{lp}(1-x-p)^{\alpha_p/2}(1-u_{out}), & \\ 1-u_{out} < u'_{dop}, & \text{Linear region,} \\ k_{sp}(1-x-p)^{\alpha_p}, & \\ 1-u_{out} \ge u'_{dop}, & \text{Saturation region,} \\ 0, & \\ x \ge 1-p, & \text{Cutoff region,} \end{cases} \quad (4)$$

where $k_{sp} = \frac{I_{D0p}}{(1-p)^{\alpha_p}}$, $k_{lp} = \frac{I_{D0p}}{u_{dop}(1-p)^{\alpha_p/2}}$, $u'_{dop} = u_{dop}\left(\frac{1-x-p}{1-p}\right)^{\frac{\alpha_p}{2}}$.

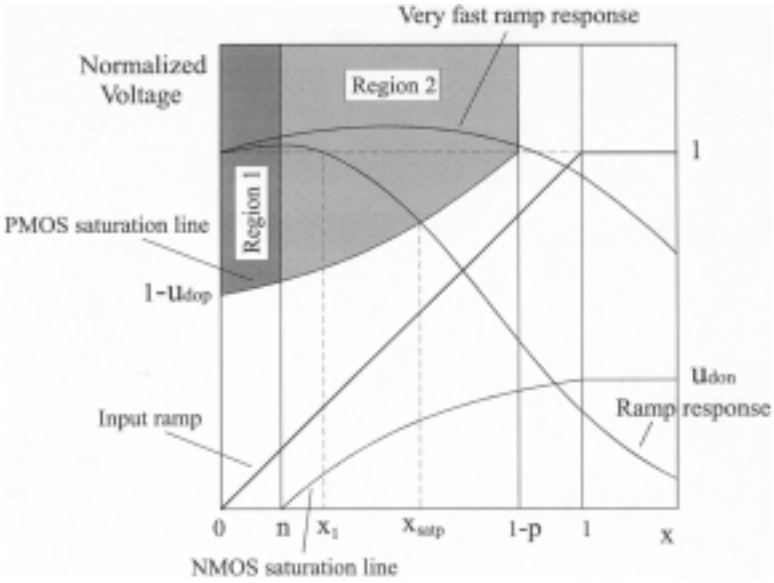


Figure 2 Operation regions of the inverter.

Short-circuit power is dissipated when a direct current path from power supply to ground is caused. Part of the charge from the input which is injected through the gate-to-drain coupling capacitance causes an overshoot at the early part of the output voltage waveform (Figure 2). During the overshoot there is no current from power supply to ground because the output voltage is greater than the supply voltage. Thus, short-circuit power is dissipated from the end of the output voltage overshoot ($x = x_1$), until the PMOS device is turned off ($x = 1 - p$). In the following, the two first operation regions (Figure 2) of the inverter are analyzed, in order to evaluate the short-circuit power dissipation.

Region 1: $0 \leq x \leq n$
Since, the NMOS transistor is off the discharge of the output node does not start in this region, which means that the end of the output voltage overshoot occurs in the next region. Thus, in this region there is no short-circuit power dissipation, but the expression of the output voltage waveform is required in order to find the initial conditions of the next region. During the overshoot the PMOS device operates in a reversed linear mode. The differential eq. (2) using the current eqs. (3) and (4) becomes

$$\frac{du_{out}}{dx} = c_m + A_{lp}(1 - x - p)^{\alpha_p/2}(1 - u_{out}), \qquad (5)$$

where $c_m = \frac{C_M}{C_L + C_M}$ and $A_{lp} = \frac{k_{lp}\tau_r}{V_{DD}(C_L + C_M)}$. In this region: $C_M = C_{gdn-overlap} + C_{gdp-overlap} + C_{gdp-channel}$.

The first term of the right part in eq. (5) corresponds to the charging current due to the coupling capacitance (C_M), which causes the major influence on the output voltage waveform in this region. Since the above differential equation cannot be solved analytically an average value of x, ($x_{av} = n/2$) is used in the expression of the PMOS current, resulting in the following solution:

$$u_{out} = 1 + c_m y_n^{-1}\left(1 - e^{-y_n x}\right), \qquad (6)$$

where

$$y_n = A_{lp}\left(1 - p - \frac{n}{2}\right)^{\frac{\alpha_p}{2}}.$$

Region 2: $n \leq x \leq x_{satp}$
The NMOS device is saturated and the PMOS device is still in the linear region. Note that the right limit of this region is the normalized time value x_{satp} (Figure 2) when the PMOS device is entering the saturation region, i.e. $1 - u_{out} = u'_{dop}$. In the special case of very fast input ramps the PMOS device is turned off after its linear region without entering saturation, i.e. $x_1 > 1 - p$ (Figure 2). In region 2 the differential eq. (2) becomes

$$\frac{du_{out}}{dx} = c_m - A_{sn}(x - n)^{\alpha_n} + A_{lp}(1 - x - p)^{\alpha_p/2}(1 - u_{out}), \qquad (7)$$

where and $A_{sn} = \frac{k_{sn}\tau_r}{V_{DD}(C_L + C_M)}$ and C_M has the same value as in region 1. The third term of the

right part in eq. (7) corresponds to the PMOS device current. Since the influence of the PMOS current on the output voltage waveform is small, two approximations concerning this term are used, in order to give a solution of eq. (7). First, an approximation of u_{out} in the expression of the PMOS current is used. The approximated $u_{out}^{'}$ is derived assuming negligible PMOS current in eq. (7),

$$u_{out}^{'} = 1 + c_m(x - n + R) - \frac{A_{sn}}{(\alpha_n + 1)}(x - n)^{\alpha_n + 1},$$

where $R = y_n^{-1}(1 - e^{-ny_n})$. Second, a constant value of x ($x_c = 0.9 \cdot (1 - p)$) in the normalized gate-source voltage of the PMOS device has been found to compensate the error of the underestimated $u_{out}^{'}$. After the above approximations the solution of eq. (7) is

$$\begin{aligned} u_{out} = {} & 1 + c_m(R - n)(1 + ny_s) \\ & + \frac{c_m y_s n^2}{2} + c_m[1 - y_s(R - n)]x \\ & - \frac{c_m y_s x^2}{2} + \frac{A_{sn}(x - n)^{\alpha_n + 1}}{(\alpha_n + 1)} \\ & \cdot \left[\frac{(x - n)y_s}{(\alpha_n + 2)} - 1\right]. \end{aligned} \quad (8)$$

where $y_s = A_{lp}[0.1 \cdot (1 - p)]^{\alpha_p/2}$. The above equation gives waveforms very close to those derived from SPICE simulations, which indicates the validity of the approximations. The resulting output waveform from eqs. (6) and (8), and the waveform which is used in both works of Sakurai and Newton (1990) and Vemuru and Scheinberg (1994) are shown in Figure 3. The latter does not include the effects of the short-circuit current and the gate-to-drain coupling capacitance. For comparison purposes, the output waveform derived from SPICE is also included in the diagram.

In order to continue the analysis for the evaluation of the short-circuit power dissipation, the calculation of the normalized time value x_{satp} and the normalized voltage value u_{satp} when the PMOS device is entering the saturation region is required. These values satisfy the PMOS saturation condition: $u_{out} = 1 - u'_{dop}$. In order to solve this equation a Taylor series expansion at the point x = 1 - n - p up to the fourth order coefficient is used, for both u_{out} and u'_{dop}. After that, the PMOS saturation condition becomes

$$\sum_{k=0}^{4} z_k x^k = 1 - \sum_{k=0}^{4} m_k[x - (1 - p - n)]^k, \quad (9)$$

where z_k and m_k are the Taylor series coefficients of u_{out} and $u_{dop}^{'}$, respectively, which are given in the Appendix. Standard ways of finding the Taylor series coefficients and the roots of a quadric equation can be found in most mathematical handbooks (Spiegel, 1968). The only root of eq. (9) which belongs in the interval $[n, 1 - p]$ is x_{satp}. The error which is introduced to the evaluation of x_{satp} due to the above method is up to 0.3%. By substituting x_{satp} in eq. (8) the normalized output voltage u_{satp} is calculated. Note that in Vemuru and Scheinberg (1994) a rough approximation for x_{satp} is used ($x_{satp} = 1 - n - p$), which results in an important error in the evaluation of the short-circuit power dissipation.

CMOS SHORT-CIRCUIT POWER DISSIPATION

As mentioned in the second section, during the overshoot of the output voltage waveform there is no current from power supply to ground because V_{out} is higher than V_{DD}. Thus, short-circuit energy is dissipated from the end of the overshoot ($x = x_1$), until the PMOS device is turned off ($x = 1 - p$). The short-circuit energy dissipation during a falling output transition is given by

$$\begin{aligned} E_{SCF} &= V_{DD} \int I_{SC} dt \\ &= V_{DD} \left[\int_{x_1}^{x_{satp}} I_p \tau_r dx + \int_{x_{satp}}^{1-p} I_p \tau_r dx \right]. \end{aligned} \quad (10)$$

The first integral cannot be solved with the expression of the PMOS device current in its linear region (eq. (4)). Thus, in this integral we use the PMOS current as given by the application of the Kirchoff's current law to the output node of the inverter (eq. (2))

$$I_p = k_{sn}(x - n)^{\alpha_n} - \frac{V_{DD} C_M}{\tau_r} + \frac{V_{DD}(C_M + C_L)}{\tau_r} \frac{du_{out}}{dx}. \quad (11)$$

The integration of eq. (10) using eq. (11) in the first integral and eq. (4) for the PMOS saturation current in the second integral, yields

$$\begin{aligned} E_{SCF} = {} & \frac{V_{DD} k_{sn} \tau_r}{(\alpha_n + 1)} \left[(x_{satp} - n)^{\alpha_n + 1} \right. \\ & \left. - (x_1 - n)^{\alpha_n + 1}\right] - V_{DD}^2 C_M (x_{satp} - x_1) \\ & + V_{DD}^2 (C_L + C_M)(u_{satp} - 1) \end{aligned}$$

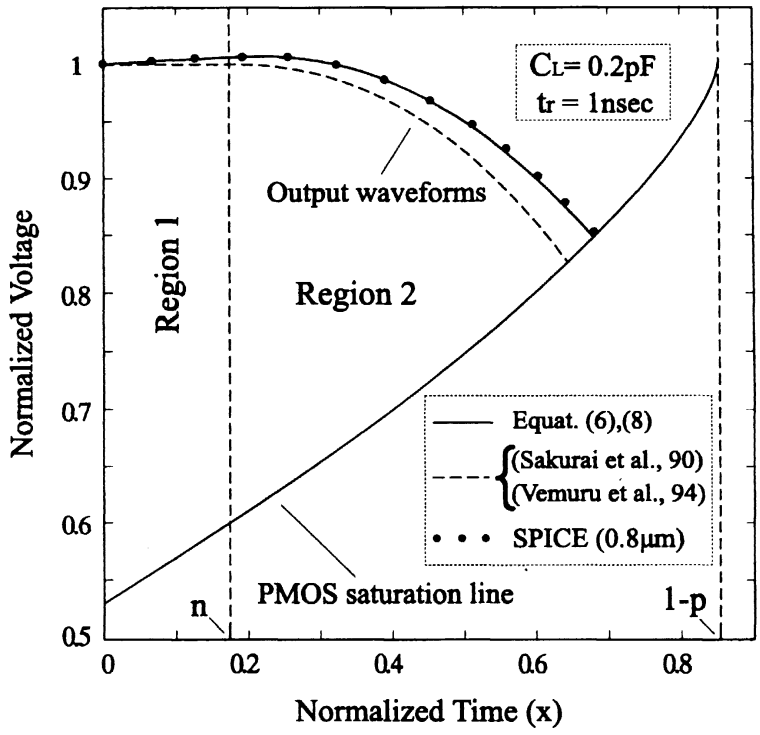


Figure 3 Inverter output waveforms for the first two operation regions.

$$+\frac{V_{DD}k_{sp}\tau_r}{(\alpha_p+1)}(1-x_{satp}-p)^{\alpha_p+1}. \qquad (12)$$

The end of the output voltage overshoot ($x = x_1$) occurs in region 2, due to the fact that the discharge of the output node, which is initially charged at V_{DD}, does not start in region 1 since the NMOS device is off. Thus, x_1 is evaluated if we set $u_{out} = 1$ in eq. (8). As in the case of x_{satp} (second section, region 2), the Taylor series expansion of u_{out} can be used (Appendix). In this case, in order to obtain better accuracy the expansion has been done at the point $x = 2n$. This results in an error in the evaluation of x_1 no greater than 0.1%.

The analysis for the evaluation of the short-circuit energy dissipation during the rising output transition is symmetrical, and results in the following formula:

$$\begin{aligned} E_{SCR} = {} & \frac{V_{DD}k_{sp}\tau_f}{(\alpha_p+1)}\left[(x_{satn}-p)^{\alpha_p+1}\right. \\ & \left.-(x_1-p)^{\alpha_p+1}\right] - V_{DD}^2 C_M (x_{satn}-x_1) \\ & -V_{DD}^2(C_L+C_M)u_{satn} \\ & +\frac{V_{DD}k_{sn}\tau_f}{(\alpha_n+1)}(1-x_{satn}-n)^{\alpha_n+1}, \end{aligned} \qquad (13)$$

where x_1 is now the normalized time at which the output voltage undershoot ends, and x_{satn}, u_{satn} are the normalized time and the normalized output voltage, respectively, when the NMOS device is entering the saturation region.

Finally, the short-circuit power dissipation P_{SC}, is given by:

$$P_{SC} = (E_{SCF} + E_{SCR})f, \qquad (14)$$

where f is the switching frequency.

RESULTS AND DISCUSSION

In Figures 4, 5, 6 and 7 the short-circuit energy dissipation during one switching cycle is plotted as a function of the input transition time. Two different CMOS process technologies of 0.8 μm and 1.2 μm, and two different output loads of 0.1 pF and 0.2 pF have been used to verify the accuracy of the presented model. The device parameters and the dimensions of both transistors are listed in Table I. The value of the supply voltage is 5 Volts. In order to achieve symmetrical inverters the widths of the transistors have been selected so as the drain currents at $V_{GS} = V_{DS} = V_{DD}$ be equal.

Results using the approaches for the evaluation of the short-circuit energy dissipation presented in Hedenstierna and Jeppson (1987, 1992), Sakurai and Newton (1990), Veendrick (1984) and Ve-

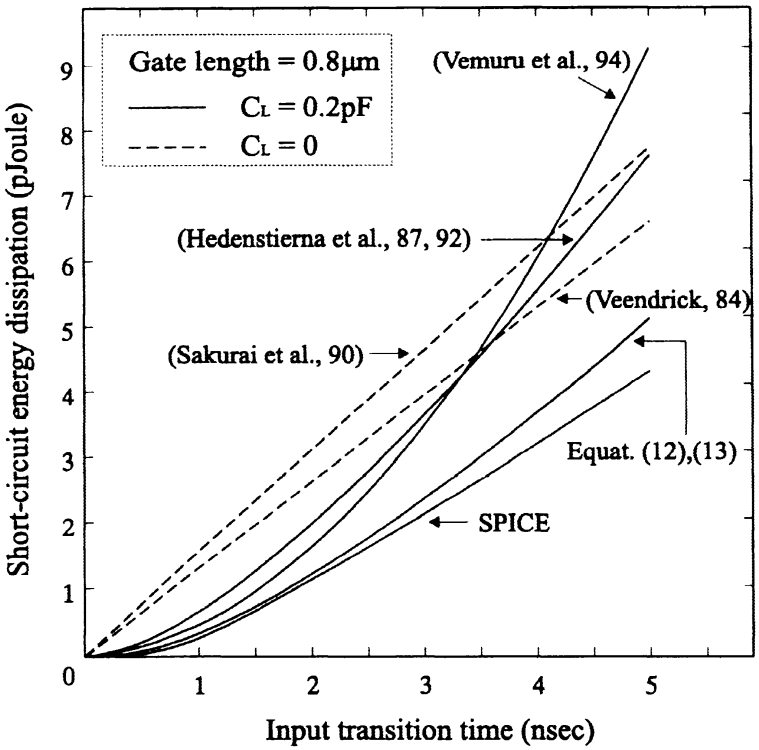


Figure 4 Short-circuit energy dissipation per switching cycle (gate length = 0.8 μm, C_L = 0.2 pF).

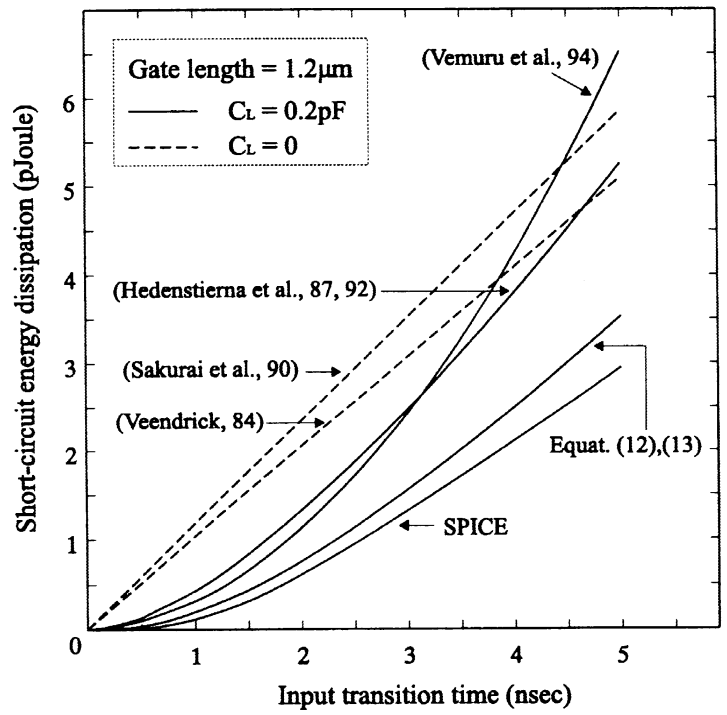


Figure 5 Short-circuit energy dissipation per switching cycle (gate length = 1.2 μm, C_L = 0.2 pF).

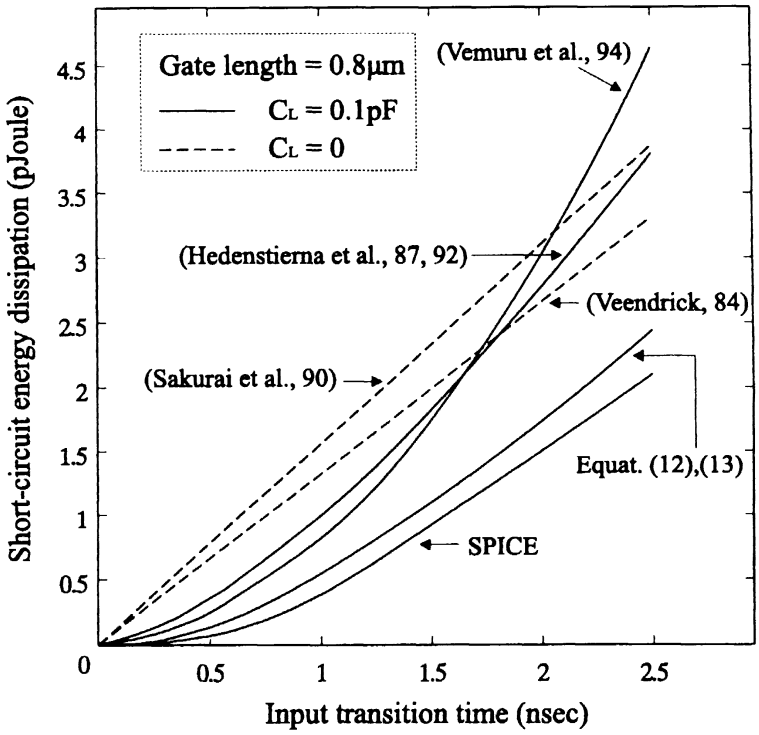


Figure 6 Short-circuit energy dissipation per switching cycle (gate length = 0.8 μm, C_L = 0.1 pF).

Table I MOSFETs parameters

Parameter	$L = 0.8$ μm		$L = 1.2$ μm	
	NMOS	PMOS	NMOS	PMOS
W (μm)	4	6.55	5	11.75
I_{D0} (mA)	1.72	1.72	1.53	1.53
$\|V_{D0}\|$ (V)	1.30	2.45	1.70	2.50
α	1.29	1.41	1.43	1.54
$\|V_{TH}\|$ (V)	0.844	0.734	0.736	0.751
C_{ox} (fF/μm^2)	2.18	2.18	1.45	1.45
C_{gdo} (fF/μm)	0.35	0.35	0.30	0.30

muru and Scheinberg (1994), are also given. Note that the results from Sakurai and Newton (1990) and Veendrick (1984) are for $C_L = 0$, due to the assumption of zero load capacitance in these approaches. It can be observed that our model gives results closer to those derived from SPICE simulations than the other methods. This occurs because the model includes the influences of the short-circuit current and the gate-to-drain coupling capacitance on the expression of the inverter output waveform. As we can see in the figures with the results, the other methods overestimate the short-circuit energy dissipation because they do not include these two effects, or they use some additional simplifications in order to evaluate the short-circuit energy dissipation. Also, some of these methods (Veendrick, 1984; Hedenstierna and Jeppson, 1987, 1992) are based on the square-law MOS model which does not reproduce the current characteristics of short-channel devices. Another advantage of our model is the use of a quite accurate method for the determination of the time where the short-circuiting transistor changes from the linear region to the saturation region.

The SPICE simulation results have been obtained by using the powermeter subcircuit proposed by Kang (1986) and Yacoub and Ku (1989), as is shown in Figure 8(a). The short-circuit energy dissipation during the falling output transition is measured by the powermeter connected between the power supply and the PMOS transistor. The short-circuit current waveform and the output of

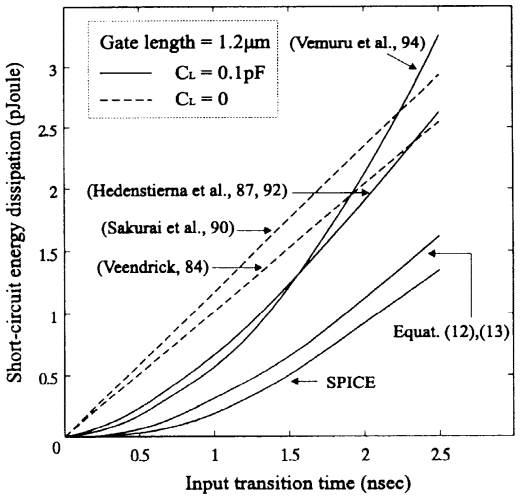


Figure 7 Short-circuit energy dissipation per switching cycle (gate length = 1.2 μm, C_L = 0.1 pF).

the powermeter during the falling output transition are shown in Figure 8(b). Short-circuit energy is dissipated in the interval $[x_1, 1-p]$ where current flows from power supply to ground. The reverse current which flows in the interval $[0, x_1]$ is due to the presence of the gate-to-drain and gate-to-source capacitance and is provided from the input (or the supply of the previous stage). Thus, its energy component is excluded from the estimation of the short-circuit dissipation. For measuring the short-circuit energy dissipation E_{SCF} during the falling output transition, two powermeter readings PM_{x_1} and $PM_{(1-p)}$ at the normalized time points x_1 and $1-p$, respectively, must be taken. Then,

$$E_{SCF} = (PM_{(1-p)} - PM_{x_1})T, \tag{15}$$

where T is the duration of measure (Kang, 1986). The measurement of the short-circuit energy dissipation during the rising output transition is performed in a similar way to the powermeter connected between the NMOS transistor and ground.

An important issue is to study the contribution of the short-circuit energy dissipation to the total energy dissipation (capacitive plus short-circuit). In Figures 9 and 10 the short-circuit energy dissipation percentage of the total energy dissipation during one switching cycle is plotted as a function of the input transition time. Two different CMOS process technologies of 0.8 μm and 1.2 μm, and two different output loads of 0.1 pF and 0.2 pF are used. The results show that the contribution of the short-circuit energy to the total energy increases when the input transition time is increased or when the capacitive load is reduced. Hence, the percentage of the short-circuit energy dissipation increases when the input signal is slow compared with the output signal. The results comparison between Figure 9 and Figure 10 indicates that the impact of the short-circuit component on the total energy is increased when the device gate lengths are reduced.

The presented short-circuit power dissipation model can be used for more complex CMOS gates, since several fast methods (Nabavi-Lishi and Rumin, 1994; Jun et al., 1989) have been proposed for reducing a CMOS gate to an equivalent inverter. Using these called "collapsing" techniques the short-circuit power dissipation of a gate can be computed quickly and accurately using the proposed inverter-based model, and without the complications associated with trying to generalize the model to complex gates. The most critical issue in gate modeling is the reduction of serial and parallel connected MOSFETs to single transistors with equivalent drivabilities.

CONCLUSION

In this paper an accurate model for the evaluation of the CMOS short-circuit power dissipation is presented. The model is based on accurate expressions for the inverter output waveform which take into account the influences of both transistor currents and the gate-to-drain coupling capacitance. Also, the velocity saturation effects of short-channel devices are included. The comparison of the results derived by the proposed approach with previously published research shows much better agreement with SPICE measurements.

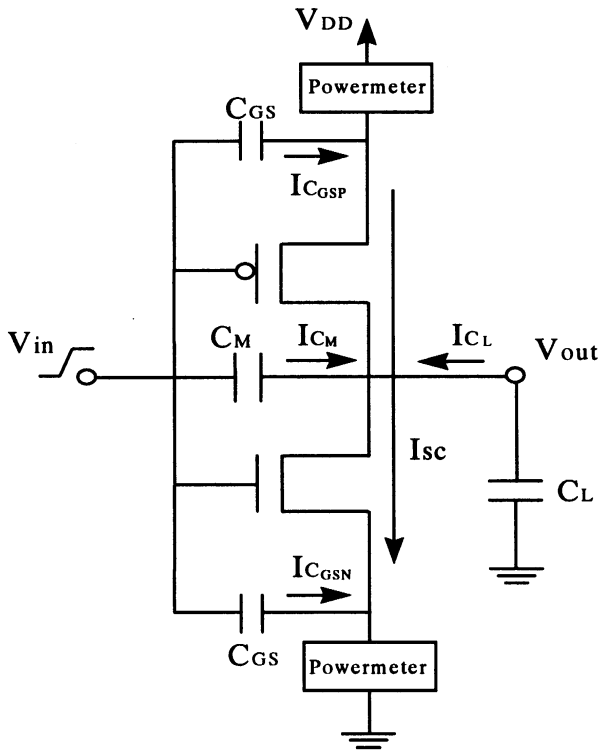
APPENDIX: TAYLOR SERIES COEFFICIENTS OF u_{out} IN REGION 2, AND u'_{dop}

In this Appendix, the coefficients of the Taylor series expansion of the normalized output voltage u_{out} in region 2 (eq. (8)) and those of the normalized voltage u'_{dop} (see PMOS current eqs. (4)), are given.

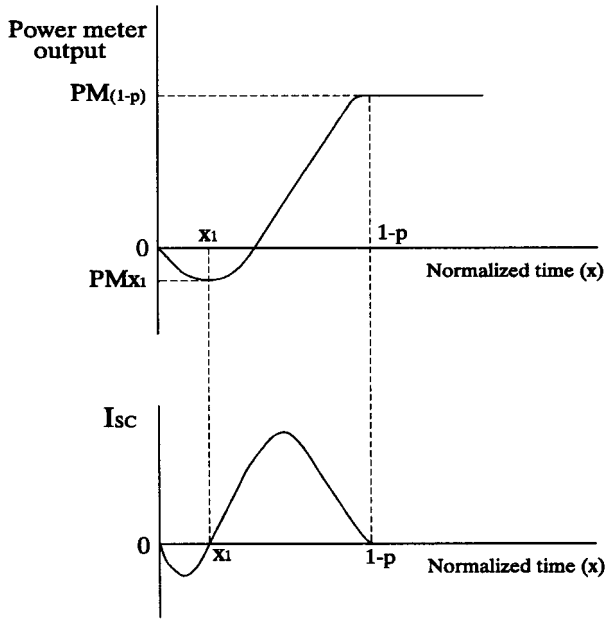
$$u_{out} = \sum_{k=0}^{4} z_k x^k,$$

where

$$z_0 = 1 + c_m(R-n)(1+ny_s) + \frac{c_m y_s n^2}{2} - d_1 f_0,$$



(a)



(b)

Figure 8 (a) Inverter currents during a falling output transition. (b) Powermeter output and short-circuit current waveforms during a falling output transition.

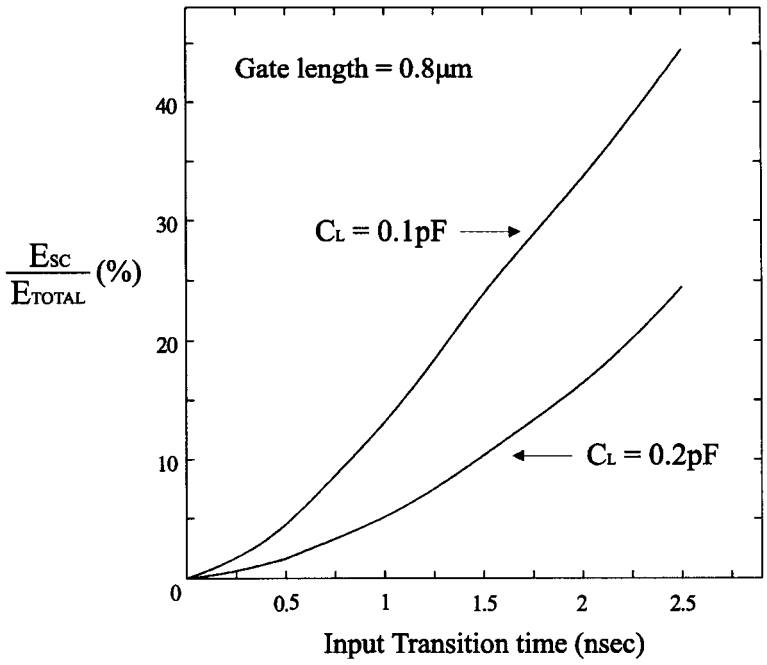


Figure 9 Short-circuit energy dissipation percentage of the total energy dissipation (gate length = 0.8 μm).

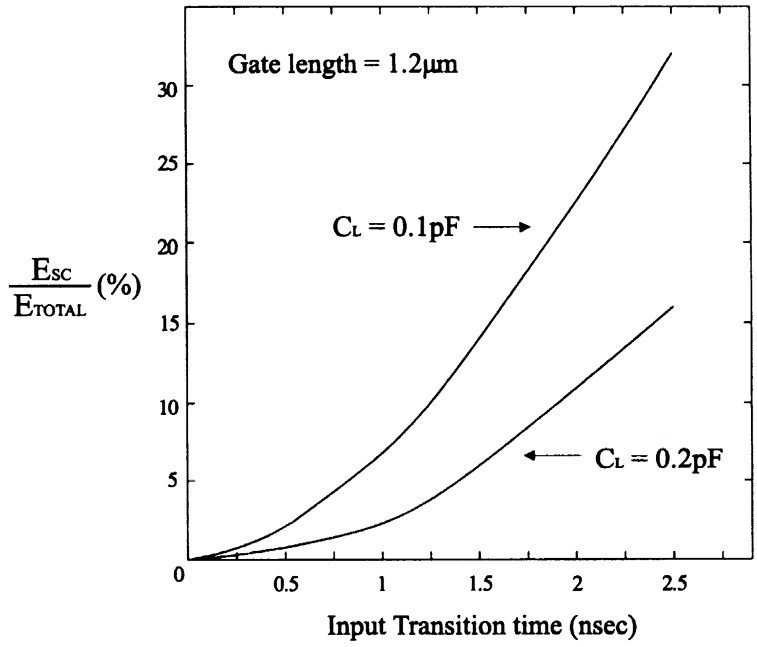


Figure 10 Short-circuit energy dissipation percentage of the total energy dissipation (gate length = 1.2 μm).

$$z_1 = c_m[1 - y_s(R - n)] + d_0 f_0 n^{-1} - d_1 f_1,$$
$$z_2 = d_0 f_1 n^{-1} - d_1 f_2 - \frac{c_m y_s}{2},$$
$$z_3 = d_0 f_2 n^{-1} - d_1 g_3,$$
$$z_4 = d_0 g_3 n^{-1},$$
$$d_0 = A_{sn} y_s n(\alpha_n + 1)^{-1}(\alpha_n + 2)^{-1},$$
$$d_1 = d_0 + A_{sn}(\alpha_n + 1)^{-1},$$
$$f_0 = g_0 - g_1\theta + g_2\theta^2 - g_3\theta^3,$$
$$f_1 = g_1 - 2g_2\theta + 3g_3\theta^2,$$
$$f_2 = g_2 - 3g_3\theta,$$
$$g_0 = (\theta - n)^{\alpha_n + 1},$$

$$g_k = \frac{(\theta - n)^{\alpha_n + 1 - k}}{k!} \prod_{i=1}^{k} (\alpha_n + 2 - i),$$

for $1 \le k \le 3$.

$$u'_{dop} = 1 - \sum_{k=0}^{4} m_k (x - \theta)^k$$

where $m_0 = u_{dop} \left(\frac{1-\theta-p}{1-p} \right)^{\alpha_p/2}$,

$$m_k = \frac{(-1)^k u_{dop}}{k!(1-p)^{\alpha_p/2}} (1 - \theta - p)^{(\alpha_p/2)-k} \cdot \prod_{i=1}^{k} \left(\frac{\alpha_p}{2} + 1 - i \right), \quad \text{for } 1 \le k \le 4.$$

Note that for the evaluation of x_{satp} (eq. (9)) $\theta = (1 - p - n)$, and for the evaluation of $x_1 \theta = 2n$. The values x_{satn} and x_1 which are used in the evaluation of the short-circuit power dissipation during the rising output transition are calculated in a similar way.

REFERENCES

Bisdounis, L., Nikolaidis, S., Koufopavlou, O., and Goutis, C.E. (1996) "Modeling the CMOS Short-Circuit Power Dissipation," *IEEE Proc. International Symposium on Circuits and Systems* 4: 469–472.

Chandrakasan, A.P., Sheng, S., and Brodersen, R.W. (1992) "Low-power CMOS Digital Design," *IEEE J. Solid-State Circuits* 27(4): 473–484.

Cherkauer, B.S., and Friedman, E.G. (1995) "A Unified Design Methodology for CMOS Tapered Buffer," *IEEE Trans. VLSI Systems* 3(1): 99–111.

Hedenstierna, N., and Jeppson, K.O. (1987) "CMOS Circuit Speed and Buffer Optimization," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems* CAD-6 (2): 270–281.

Hedenstierna, N., and Jeppson, K.O. (1993) "Comments on 'A Module Generator for Optimized CMOS Buffers'," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems* 12(1): 180–181.

Hirata, A., Onodera, H., and Tamaru, K. (1996) "Estimation of Short-Circuit Power Dissipation and its Influence on Propagation Delay for Static CMOS gates," *IEEE Proc. International Symposium on Circuits and Systems* 4: 751–754.

Jeppson, K.O. (1994) "Modeling the Influence of the Transistor Gain Ratio, and the Input-to-output Coupling Capacitance on the CMOS Inverter Delay," *IEEE J. Solid-State Circuits* 29(6): 646–654.

Jun, Y.H., Jun, K., and Park, S.B. (1989) "An Accurate and Efficient Delay Time Modeling for MOS Logic Circuits Using Polynomial Approximation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems* 8(9): 1027–1032.

Kang, S.M. (1986) "Accurate Simulation of Power Dissipation in VLSI Circuits," *IEEE J. Solid-State Circuits* SC-21(5): 889–891.

Kayssi, A.I., Sakallah, K.A., and Burks, T.M. (1992) "Analytical Transient Response of CMOS Inverters," *IEEE Trans. Circuits and Systems-I* 39(1):42–45.

Nabavi-Lishi, A., and Rumin, N.C. (1994) "Inverter Models of CMOS Gates for Supply Current and Delay Evaluation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems* 13(10): 1271–1279.

Sakurai, T., and Newton, A.R. (1990) "Alpha-power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE J. Solid-State Circuits* 25(2): 584–594.

Sakurai, T., and Newton, A.R. (1991) "A Simple MOSFET Model for Circuit Analysis," *IEEE Trans. Electron Devices* 38(4): 887–894.

Shichman, H., and Hodges, D.A. (1968) "Modeling and Simulation of Insulated-gate Field-Effect Transistor Switching Circuits," *IEEE J. Solid-State Circuits* SC-3(9): 285–289.

Spiegel, M.R. (1968) *Mathematical Handbook of Formulas and Tables*, McGraw-Hill, Schaum's Outline Series, New York, pp. 32–33 & 110.

Turgis, S., Azemard, N., and Auvergne, D. (1995) "Explicit Evaluation of Short-circuit Power Dissipation for CMOS Logic Structures," *Proc. International Symposium on Low-Power Design* 129–134.

Veendrick, H.J.M. (1984) "Short-circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits," *IEEE J. Solid-State Circuits* SC-19(4): 468–473.

Vemuru, S.R., and Scheinberg, N. (1994) "Short-circuit Power Dissipation Estimation for CMOS Logic Gates," *IEEE Trans. Circuits and Systems-I* 41(11): 762–765.

Weste, N.H.E., Eshraghian, K. (1993) *Principles of CMOS VLSI Design: A Systems Perspective*, McGraw-Hill, New York, pp. 183–191.

Yacoub, G.Y., and Ku, W.H. (1989) "An Enhanced Technique for Simulating short-circuit Power Dissipation," *IEEE J. Solid-State Circuits* 24(6): 844–847.