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ANALYTICAL MODELING OF OVERSHOOTING EFFECT IN SUB-100 nm CMOS INVERTERS*

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Modeling of CMOS inverters and consequently, CMOS gates, is a critical task for improving accuracy and speed of simulation in modern sub-100 nm digital circuits. One of the key factors that determine the operation of a CMOS structure is the influence of the input-to-output coupling capacitance, also called overshooting effect. In this paper, an analytical model for this effect is presented, that computes the time period which is necessary to eliminate the extra output charge transferred through the input-to-output capacitance at the beginning of the switching process in a CMOS inverter. In addition, the maximum or minimum output voltage (depending on the considered edge) is analytically computed. The derived model is based on analytical expressions of the CMOS inverter output voltage waveform, which include the influences of both transistor currents and the input-to-output (gate-to-drain) coupling and load capacitances. An accurate version of the alpha-power law MOSFET model is used to relate the terminal voltages to the drain current in sub-100 nm devices, with an extension for varying transistor widths. The resulting model also accounts for the influences of input voltage transition time, transistors' sizes, as well as device carrier velocity saturation and narrow-width effects. The results produced by the presented model for three sub-100 nm CMOS technologies, several input voltage transition times, capacitive loads and device sizes, show very good agreement with BSIM4 HSPICE simulations.

Keywords: CMOS inverters; nanometer MOSFETs; circuit modeling; circuit simulation; timing analysis; computer-aided design (CAD).

1. Introduction

To improve the design time of digital circuits and the accuracy of their simulation process, computer-aided design (CAD) tools have to include fast and accurate models for the estimation of circuits delay and energy dissipation.[1] Much of previous research has addressed the issue of delay and energy dissipation estimation of CMOS inverters.[2–14] The importance of modeling delay and energy of CMOS inverters comes from the fact that the clock distribution networks and busses in digital

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integrated circuits are based on inverters or inverter-like circuits which have to be carefully modeled, since these circuits account for a great fraction of circuits' delay and energy dissipation.[15] Another equally important reason to obtain accurate models for the inverter delay and energy dissipation is that several methods for reducing CMOS gates to equivalent inverters, have been proposed.[9,16,17]

Traditionally, delay models of CMOS structures are considered the influences of transistors' sizes, input voltage transition time and output load.[2,4,18] Recently, several techniques have been proposed to include the influence of the input-to-output coupling capacitance.[8,10,13,14] However, the used approximations lead to inaccuracies in what concerns the computation of the overshoot time period, i.e., the time period which is necessary to eliminate the extra output charge transferred through the input-to-output capacitance at the beginning of the inverter switching process. In addition, during switching of a CMOS structure, a direct path from power supply to ground is established, resulting in short-circuit energy dissipation that accounts for a considerable part of the total energy dissipation.[1,5,19] The overshoot time period has a significant role in the computation of the short-circuit energy dissipation.[5,7,9,10,12] Therefore, in order to produce fast and accurate models for both CMOS delay and energy dissipation, it is important to derive an accurate analytical model of the overshooting effect.

In this paper, an analytical model for the overshooting effect due to input-to-output coupling capacitance in sub-100 nm CMOS buffers is proposed. Closed-form expressions for the overshoot time period as well as for the maximum or minimum output voltage (depending on the considered edge) are derived, that can be used by several existing CMOS delay and energy dissipation models. The proposed model is based on a version of the alpha-power law MOSFET model[11] that uses an accurate device drain current expression in the triode region, rather that the linear expression proposed by Sakurai and Newton in 1990.[4] In addition, an extension of the device model is used to cope with narrow-width effects of sub-100 nm devices.[20] For the derivation of the desired closed-form expressions, analytical expressions of the output voltage waveform in the related operating regions are used. These expressions take into account the drain currents of both transistors and the influence of the gate-to-drain coupling capacitance, and they are valid for a wide range of input voltage transition times, supply voltages, output loads and device sizes.

Previous attempts to model the overshooting effect of a CMOS inverter, Turgis and Auvergne[7] used a simplified MOSFET model for submicrometer devices, and the overshoot time period was computed by neglecting the short-circuit current, resulting in evaluation uncertainties especially for fast inputs. Hamoui and Rumin,[10] initially computed the time at which the short-circuiting transistor of the inverter enters saturation. And by using a piecewise-linear approximation of the short-circuit current, they related the overshoot time period with this time value. However, their model uses numerical procedures and the assumption of negligible short-circuit current for the computation of the time at which the short-circuiting transistor

enters saturation. Rossello and Segura[12] computed the time at which the overshoot current takes its maximum value, and related the overshoot time period to this value, by using an empirical linear relationship based on simulation data. The time at which the overshoot current is at its maximum was obtained by neglecting the influence of the short-circuit current and by using approximations for the saturation voltage and current of the inverter's load transistor. A similar approach has been proposed by Huang *et al.*,[14] where the overshoot time period is related to the time at which the inverter output voltage is at its maximum or minimum (depending on the considered edge), by assuming a linear load capacitance current. Additional assumptions were used, such as the simplified expression for the short-circuit current, negligible output voltage change rate during the overshoot period, linear load transistor drain current and the approximation that the maximum or minimum (depending on the considered edge) output voltage occurs at the time at which the inverter's load transistor is turned-on.

The rest of the paper is organized as follows. The influence of the overshooting effect on the delay and short-circuit energy dissipation of CMOS buffers is analyzed in Sec. 2. In Sec. 3, the used MOSFET model for sub-100 nm devices is described. The proposed method for the evaluation of the overshoot time period and the maximum output voltage is presented in Sec. 4. Results and comparisons with previous works and BSIM4[21] HSPICE[22] simulations are given and discussed in Sec. 5. This paper is concluded in Sec. 6.

2. Overshooting Effect Influence on CMOS Delay and Energy Dissipation

Figure 1 shows the CMOS inverter under a rising input voltage. The equivalent input-to-output coupling capacitance (C_M) accounts for the sum of the gate-to-drain capacitances of both transistors, which consists of the gate-to-drain overlap capacitance and a part of the gate-to-channel capacitance. It is calculated using the parameters C_{ox} (gate-oxide capacitance per unit area) and C_{gdo} (gate-to-drain

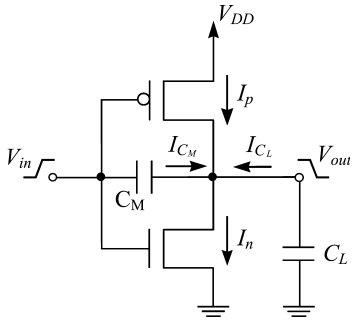


Fig. 1. The CMOS inverter.

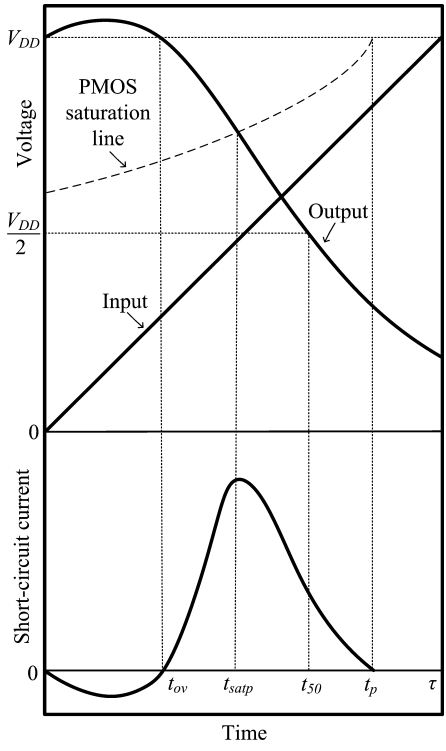


Fig. 2. Output voltage and short-circuit current of the CMOS inverter for a rising input voltage.

overlap capacitance per unit channel width).[1] The load capacitance (C_L) consists of the inverter drain junction capacitances, the gate capacitances of fan-out gates and the interconnect capacitance. In Fig. 2, the output voltage and the short-circuit current (PMOS drain current) of the inverter are shown for a rising input voltage.

The propagation delay of the CMOS inverter is traditionally given by

$$D = t_{50} - \frac{\tau}{2}, \tag{1}$$

where t_{50} is the time period for the output voltage to reach 50% of the supply voltage (V_{DD}) and τ is the input voltage transition time. A significant part of t_{50} accounts for the overshoot time period (t_{ov}), so neglecting the influence of C_M will lead to significant inaccuracies regarding the estimation of the delay in CMOS structures.

Figure 3 shows the overshoot time period (t_{ov}) and time period for the output voltage to reach 50% of the supply voltage (t_{50}), as a function of input voltage transition time in a 90-nm CMOS inverter. The illustrated data have been produced by the BSIM4 HSPICE simulations of a 90-nm CMOS inverter. The transistor model parameters have been extracted using the tool that is available in Predictive Technology Model[23] website.[24] It can be observed that the contribution of t_{ov} to t_{50} is about 30−65%, and that this contribution is more significant for fast inputs.

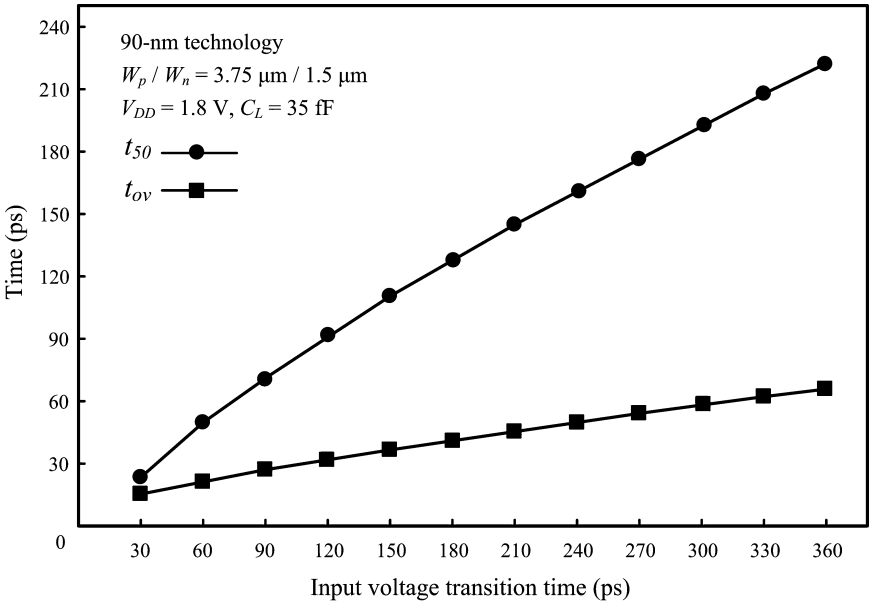


Fig. 3. Overshoot time period (t_{ov}) and time period for the output voltage to reach 50% of the supply voltage (t_{50}), as a function of input voltage transition time in a CMOS inverter.

As mentioned in Sec. 1, during switching of the CMOS inverter, a direct path from the power supply to the ground is established, resulting in short-circuit energy dissipation that accounts for a considerable part of the total energy dissipation.[1,5,19] The short-circuit energy dissipation for a rising input transition of a CMOS inverter is commonly given by

$$E_{sc} = V_{DD} \int_{t_{ov}}^{t_p} I_p dt = V_{DD} \int_{t_{ov}}^{t_{satp}} I_p dt + V_{DD} \int_{t_{satp}}^{t_p} I_p dt \,, \tag{2}$$

where t_{satp} is the time at which the short-circuiting transistor (PMOS) enters its saturation region, and t_p is the time at which the PMOS transistor is turned-off (Fig. 2). Figure 4, shows the short-circuit energy dissipation per transition (E_{sc}) with and without the influence of transistors' gate capacitance, as a function of input voltage transition time in a 90-nm CMOS inverter. The curve that takes into account the transistors' gate capacitance has been obtained by the BSIM4 HSPICE simulations, while for the second curve, an accurate analytical model[9] has been used by excluding the influence of gate capacitances and consequently the influence of C_M. Based on the results of Fig. 4, it is found that the short-circuit energy dissipation measured in an inverter having gate-to-drain capacitance, that is the real CMOS inverter, is about 10−50% smaller than that computed in an inverter neglecting the influence of gate-to-drain capacitance. As in the case of the delay the influence of

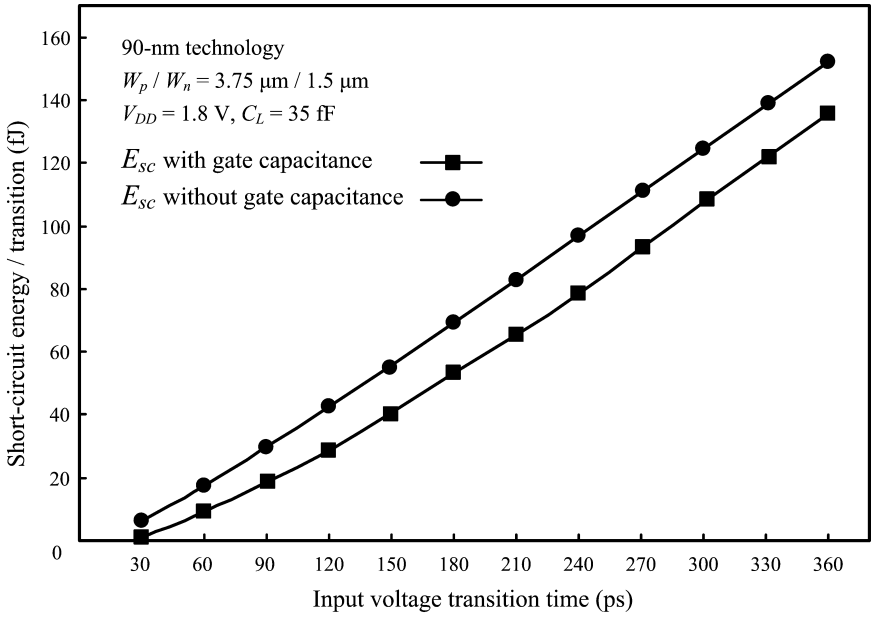


Fig. 4. Short-circuit energy dissipation per transition (E_{sc}) with and without the influence of transistors' gate capacitance, as a function of input voltage transition time in a CMOS inverter.

C_M is more significant for fast inputs. The short-circuit energy dissipation for a rising input voltage is the energy of the current from the power supply (Fig. 1). In fact, the current through the PMOS device includes a non-short-circuit current component, which is the current flowing from the output node to the supply node during the overshoot of the output signal (i.e., when $V_{\text{out}} > V_{DD}$). As shown in Fig. 2, during the output signal overshoot the current through the PMOS device is negative, and this is obviously due to the current flowing from the output node to the supply node, the presence of which leads to reduced short-circuit energy dissipation, in comparison with that dissipated in the case where the influence of the gate-to-drain coupling capacitance is not taken into account.

Therefore, in order to avoid inaccuracies in estimating the CMOS delay and short-circuit energy dissipation, it is necessary to develop an accurate and efficient analytical model for the overshooting effect. Such model can be easily incorporated in developed CMOS delay and short-circuit energy dissipation models (such as those presented in Refs. 5–14). From the practical point of view, improved analytical delay and energy dissipation models can be applied to various types of simulation (i.e., fast-timing simulation, switch-level and gate-level timing, and mixed-mode simulation), subcircuits timing/energy analysis and characterization, as well as to transistor sizing. Examples of application of analytical models in fast-timing and gate-level simulation are the ILLIADS[25,26] and HALOTIS[27] tools, respectively. The main

advantage of the analytical modeling approach is that it does not require pre-simulation such as tabular methods or empirical equation techniques, in order to improve the simulation speed. On the other hand, since analytical models for circuit primitives (like the CMOS inverter) preserve the nonlinearity of the devices, they incorporate the impact of modern technologies' effects, resulting in high accuracy without the need for computational expensive iterations and numerical methods used in SPICE-like circuit simulators.

3. MOSFET Model for Sub-100 nm Devices

The development of analytical modeling of timing or energy parameters for circuit primitives, like the CMOS inverter, requires a MOSFET model that combines accuracy, by including the influences of the main modern technologies' effects, and simplicity, to provide the ability to derive closed-form expressions. The adopted MOSFET model takes into account the influence of the main effects of deep-sub-micrometer and nanometer devices, while neglecting secondary effects in order to preserve the required simplicity. Therefore, before presenting the analytical model for the overshooting effect, it is reasonable to describe the MOSFET model that is used for expressing the transistors' drain current. It is obvious that the accuracy of the drain current model for sub-100 nm devices determines to a large extent the accuracy of the overshooting effect model. For the transistors' drain current, the following accurate and simple version of the alpha-power law MOSFET model is used.[11] The parameters of the adopted modified alpha-power MOSFET model are computed by suitable fitting of MOSFET characteristics, produced by simulation using BSIM4 predictive models.[23,24]

For $V_{DS} > V'_{DO}$ (saturation region):

$$I_D = B(V_{GS} - V_T)^{\alpha}. \tag{3}$$

For $V_{DS} \leq V'_{DO}$ (saturation region):

$$I_D = B(V_{GS} - V_T)^{\alpha}\left(2 - \frac{V_{DS}}{V'_{DO}}\right)\frac{V_{DS}}{V'_{DO}}, \tag{4}$$

where

$$V'_{DO} = K(V_{GS} - V_T)^{\alpha/2} \tag{5}$$

α: velocity saturation index (extracted as mentioned in Ref. 4), V'_{DO}: drain-source saturation voltage, B: transconductance parameter, V_T: threshold voltage. B is calculated from Eq. (3) by using the drain current extracted from the output MOSFET characteristics for $V_{GS} = V_{DD}$ and $V_{DS} = 3/4V_{DD}$ (for the NMOS devices), $V_{DS} = 4/5V_{DD}$ (for the PMOS device), in order to compensate for inaccuracies due to channel length modulation. B is extracted for the minimum device width, and in order to extend the model for higher device channel widths (W), the

following equation is used[20]:

$$B = \beta_1 + \beta_2 W + \beta_3 W^2 \,, \tag{6}$$

where the coefficients β_i are determined by fitting a quadratic plot to the B vs W plot (once for a given technology). K is computed by combining Eqs. (3)–(5) and using the coordinates (I_{DS}, V_{DS}) of an output I–V characteristics point close to the middle of the triode region (for $V_{GS} = V_{DD}$):

$$K = \frac{BV_{DS}(V_{DD} - V_T)^{a/2} + \sqrt{BV_{DS}^2[B(V_{DD} - V_T)^a - I_{DS}]}}{I_{DS}} \,. \tag{7}$$

The used MOSFET model is more accurate for sub-100 nm devices than the classic alpha-power law model[4] that uses linear drain current at the triode region, as shown in Fig. 5, in which points A and C used for the extraction of the parameters K and B, respectively, are also indicated.

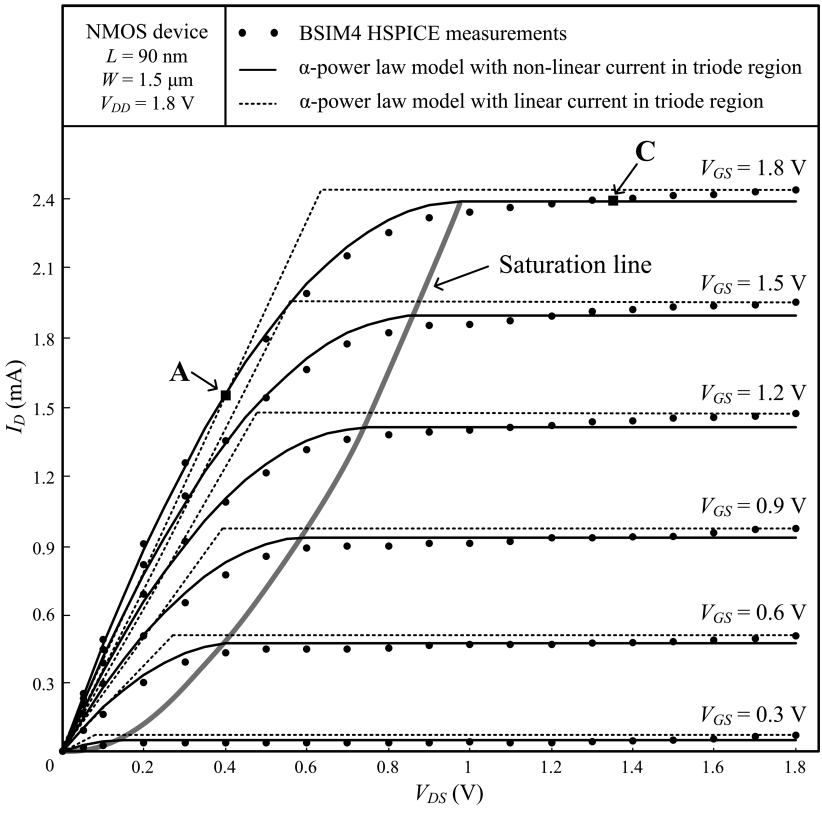


Fig. 5. 90-nm NMOS device I–V plots.

4. Overshooting Effect Modeling

The derivations presented in the following are for a rising input voltage ramp: $V_{\text{in}} = V_{DD}\ (t/\tau)$ for $0 \le t \le \tau, V_{\text{in}} = 0$ for $t \le 0$ and $V_{\text{in}} = V_{DD}$ for $t \ge \tau$, where τ is the input voltage rise time. The analysis for a falling input is symmetrical. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter (Fig. 1), taking into account the current through the gate-to-drain coupling capacitance (C_M) is written as

$$C_L \frac{dV_{\text{out}}}{dt} = C_M \left(\frac{dV_{\text{in}}}{dt} - \frac{dV_{\text{out}}}{dt} \right) + I_p - I_n \,. \tag{8}$$

For the expressions of the transistor currents, the MOSFET model presented in the previous section is used. After normalizing voltages with respect to the supply voltage (V_{DD}), i.e., $u_{\text{in}} = V_{\text{in}}/V_{DD}$, $u_{\text{out}} = V_{\text{out}}/V_{DD}$, $n = V_{TN}/V_{DD}$, $p = |V_{TP}|/V_{DD}$, $u'_{don} = V'_{DON}/V_{DD}$, $u'_{dop} = V'_{DOP}/V_{DD}$, and using the variable $x = t/\tau$, the PMOS device current in the linear region ($1 - u_{\text{out}} < u'_{dop}$) is given by the following equation:

$$I_p = k_{lp1}(1 - x - p)^{\alpha_p/2}(1 - u_{\text{out}}) - k_{lp2}(1 - u_{\text{out}})^2 \,, \tag{9}$$

where $k_{lp1} = \frac{2B_P V_{DD}^{(\alpha_p+2)/2}}{K_P}$ and $k_{lp2} = \frac{B_P V_{DD}^2}{K_P^2}$.

The NMOS device current in the saturation region ($u_{\text{out}} \ge u'_{don}$) is given by

$$I_n = k_{sn}(x - n)^{\alpha_n} \,, \quad \text{where } k_{sn} = B_N V_{DD}^{\alpha_n} \,. \tag{10}$$

After the normalization, the differential equation (8) becomes

$$\frac{du_{\text{out}}}{dx} = c_m + \frac{(I_p - I_n)\tau}{(C_L + C_M)V_{DD}}, \quad \text{where } c_m = \frac{C_M}{C_L + C_M} \,. \tag{11}$$

For $0 \le x \le n$ (Fig. 2) the NMOS transistor is off and the PMOS transistor is in the linear region. For $n < x \le x_{ov}$, the NMOS transistor is saturated and the PMOS transistor is still in the linear region. Part of the charge from the input which injected through the gate-to-drain coupling capacitance causes an overshoot at the early part of the output voltage waveform. During the overshoot, there is no current from power supply to ground because the output voltage is greater than the supply voltage. In order to accurately model the overshooting effect, the derivation of analytical expressions of the inverter output waveform in the above periods is required.

For $0 \le x \le n$, the differential equation (11) cannot be solved analytically. In this region of operation, the main influence on the output voltage waveform is due to the charge from the input which is injected through the gate-to-drain coupling capacitance, while the influence of the PMOS transistor current is quite small. So if one applies careful approximations in the expression of the PMOS transistor current, the accuracy of the resulting output voltage expression will not be affected. Therefore, for $0 \le x \le n$, an average value of x ($x = n/2$) is used in the first term of PMOS

current (Eq. (9)). The normalized time point $x = n/2$ corresponds to the middle of the related inverter operating region, so it is reasonable to use it, in order that the differential equation (11) be solved analytically. Note that the parameter n is between 0.15 and 0.25 for typical sub-100 nm technologies.

In addition, an approximated expression for u_{out} ($u_{\text{out}} = 1 + c_m x$) is used in the quadratic term of the PMOS current. This approximated expression takes into account only the charge through the gate-to-drain coupling capacitance, but it is used only in the quadratic term of the PMOS transistor current [i.e., $(1 - u_{\text{out}})^2$] and not within the whole expression of the PMOS transistor current. The approximation is reasonable, since (as mentioned earlier) in this operating region, the main influence on the output voltage waveform is due to the charge injected through the gate-to-drain coupling capacitance. Moreover, the charge contributed by the quadratic term of the PMOS transistor current is very small due to the small values of the PMOS transistor normalized drain-source voltage (i.e., $1 - u_{\text{out}}$) in this operating region. After the adoption of both approximations, u_{out} is given as

$$u_{\text{out}} = 1 + \frac{c_m}{C^3 A_{lp1}^3}\left[2A_{lp2}c_m(D-1) + 2CA_{lp1}A_{lp2}c_m x + C^2 A_{lp1}^2(1 - D - A_{lp2}c_m x^2)\right], \tag{12}$$

where $C = (1 - p - \frac{n}{2})^{\alpha_p/2}$, $D = \exp[-CA_{lp1}x]$, and $A_{lpi} = \frac{\tau k_{lpi}}{V_{DD}(C_L + C_M)}$.

In Fig. 6, output voltage waveforms derived by Eq. (12) are compared with those produced by HSPICE BSIM4 simulations. As shown, the accuracy degradation due to adopted approximations is limited.

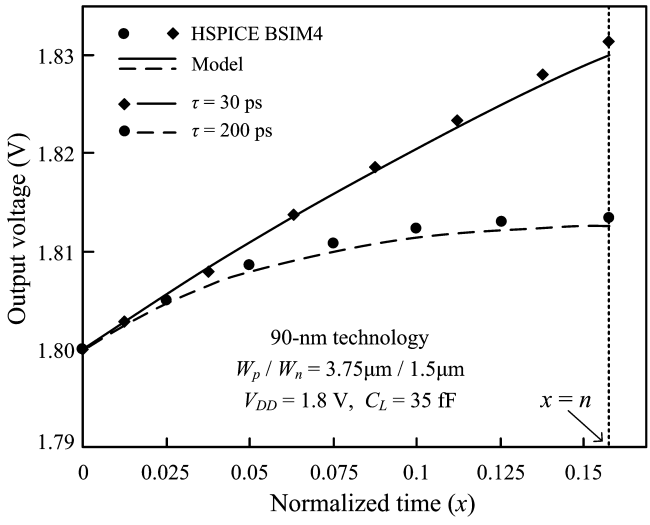


Fig. 6. Comparison of output voltage waveforms derived by Eq. (12) (for $0 \le x \le n$) with those produced by HSPICE BSIM4 simulations, for two different input transition times.

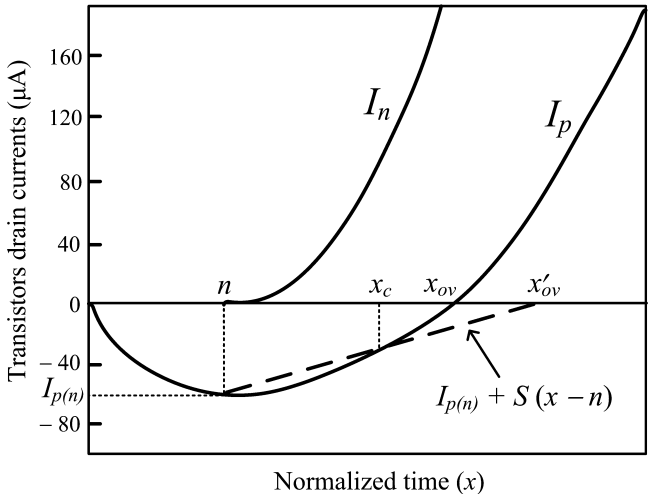


Fig. 7. Transistors drain currents during the early part of inverter switching process. The linear approximation of the PMOS current in order to obtain an output voltage waveform expression for $n < x \leq x_{ov}$ is indicated.

In order to obtain an expression of the output voltage waveform for $n < x \leq x_{ov}$, the PMOS current is approximated by a linear function of x (Fig. 7):

$$I_p = I_{p(n)} + S(x - n) \tag{13}$$

$I_{p(n)}$ is calculated by Eq. (9) for $x = n$ and $u_{\text{out}} = u_n \cdot u_n$ is calculated by Eq. (12) for $x = n$.

The current slope S is computed by equating the PMOS current in the linear region (Eq. (9)) with the approximated one (Eq. (13)), at the normalized time point: $x_c = (n + x'_{ov})/2$. x'_{ov} is the normalized time value at which the output voltage overshoot finishes with the assumption of negligible short-circuit (PMOS) current. The analytical calculation of both S and x'_{ov} is given in App. A. By using the linear approximation of the PMOS current, the differential equation (11) is solved and the output voltage waveform for $n < x \leq x_{ov}$, is described by

$$u_{\text{out}} = u_n + (x - n)c_m + dI_{p(n)}(x - n) + \frac{dS(x - n)^2}{2} - \frac{A_{sn}(x - n)^{a_n + 1}}{a_n + 1}\,, \tag{14}$$

where $d = \frac{\tau}{V_{DD}(C_L + C_M)}$ and $A_{sn} = \frac{\tau k_{sn}}{V_{DD}(C_L + C_M)}$.

The normalized time value x_{ov}, satisfies the condition $u_{\text{out}} = 1$, since it corresponds to the end of the output voltage overshoot ($V_{\text{out}} = V_{DD}$). In order to solve this equation, a Taylor series expansion of u_{out} around the point x'_{ov}, up to the second-order coefficient, is used. After that we obtain the normalized time value x_{ov}:

$$x_{ov} = \frac{-y_1 - \sqrt{y_1^2 + 4y_2 - 4y_0 y_2}}{2y_2}, \tag{15}$$

where

$$y_0 = u_n + \left(\frac{Sdn}{2} - c_m - dI_{p(n)}\right)n - A_{sn}(x'_{ov} - n)^{\alpha_n}\left[\frac{x'_{ov} - n}{a_n + 1} + \frac{a_n x'^2_{ov}}{2(x'_{ov} - n)} - x'_{ov}\right],$$

$$y_1 = c_m + (I_{p(n)} - Sn)d - A_{sn}(x'_{ov} - n)^{\alpha_n - 1}(x'_{ov} - n - a_n x'_{ov}),$$

$$y_2 = \frac{dS}{2} - \frac{A_{sn}a_n(x'_{ov} - n)^{\alpha_n - 1}}{2}.$$

Consequently, the overshoot time period t_{ov} is given by

$$t_{ov} = x_{ov}\tau. \tag{16}$$

When $x < n$, due to the charge from the input injected through the gate-to-drain capacitance, the inverter output node voltage becomes higher than V_{DD}. The PMOS drain current gradates this effect, since it tends to lead the output node to V_{DD}. Starting from the normalized time value $x = n$, the NMOS drain current is gradually increased, the current charging the output node becomes zero in a relatively short period of time, and the discharge of the output node is started. Therefore, the output voltage of the inverter reaches its maximum value within the normalized time interval $n < x < x_{ov}$. The normalized time value ($x_{\max}$) in which the maximum output voltage is reached, is computed by the following equation:

$$\begin{aligned}\frac{du_{\text{out}}}{dx} = 0 &\overset{(11)}{\Rightarrow} c_m + \frac{(I_p - I_n)\tau}{(C_L + C_M)V_{DD}} \\ = 0 &\underset{(13)}{\overset{(10)}{\Rightarrow}} c_m - A_{sn}(x - n)^{\alpha_n} + [I_{p(n)} + S(x - n)]d = 0.\end{aligned} \tag{17}$$

To avoid numerical procedures, α_n is approximated with 1, and an accurate solution for $x_{\max}$ is obtained:

$$x_{\max} = \frac{dnS - dI_{p(n)} - nA_{sn} - c_m}{dS - A_{sn}}. \tag{18}$$

Note that, the velocity saturation index (α) takes the values between 1 and 2, and as the technology scales down, α is moving close to 1. For example, α_n is between 1.03 and 1.04 for the three sub-100 nm technologies (90 nm, 65 nm, 45 nm) that are used in the next section for the evaluation of the proposed model results. For the PMOS transistor of the used technologies, the values of α are higher (between 1.2 and 1.3). An alternative method in order to solve the corresponding equation analytically, while still avoiding numerical procedures is to use a Taylor-series expansion of the term $A_{sn}(x - n)^{a_n}$, up to the second order coefficient, around the point $x = (n + x_{ov})/2$. However, test results have shown that the improvement of the model accuracy, in what concerns the following computation of the inverter maximum output voltage, is limited.

By substituting $x_{\max}$ into Eq. (14), the maximum output voltage value ($V_{\max}$) is obtained:

$$u_{\max} = u_n + (x_{\max} - n)c_m + dI_{p(n)}(x_{\max} - n) + \frac{dS(x_{\max} - n)^2}{2} - \frac{A_{sn}(x_{\max} - n)^{a_n+1}}{a_n + 1}, \tag{19}$$

$$V_{\max} = V_{DD} u_{\max}. \tag{20}$$

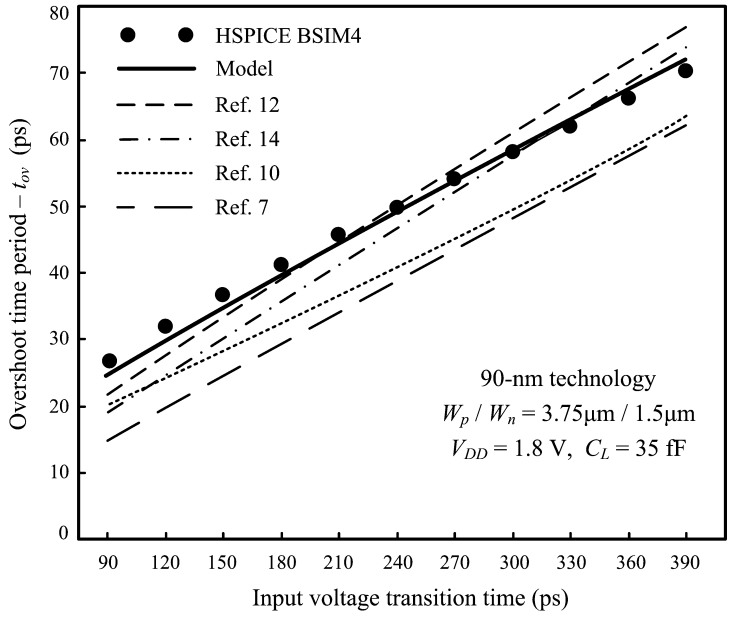
Note that, for slow inputs, the influence of the short-circuiting transistor (PMOS) drain current is increased, leading $x_{\max}$ to approach the normalized time value n.

5. Model Validation

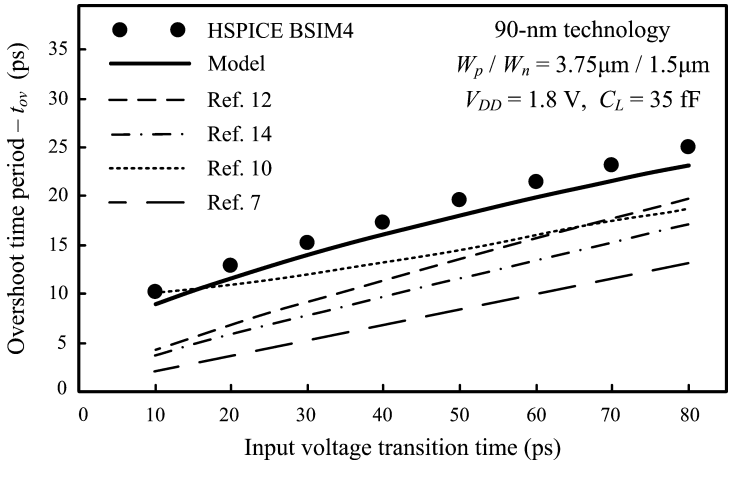
In this section, the accuracy of the proposed model is illustrated by applying it to CMOS inverters. The transistor model parameters used to obtain the presented results of BSIM4[21] HSPICE[22] simulations have been extracted by the available tool in the Predictive Technology Model[23] website.[24]

In Fig. 8, the overshoot time period during a rising input voltage transition is plotted as a function of the input voltage transition time. Figure 8(a) concerns slow input voltage transitions, while Fig. 8(b) concerns fast input voltage transitions. A 90-nm CMOS process technology has been used with a supply voltage of 1.8 V. In the inverter under test, the ratio of PMOS transistor width to NMOS transistor width was $W_p/W_n = 3.75\,\mu\text{m}/1.5\,\mu\text{m}$ and the output load was equal to 35 fF (about three equally sized inverters). Results using the models for the evaluation of the overshoot time period presented by Turgis and Auvergne,[7] Hamoui and Rumin,[10] Rossello and Segura,[12] and Huang *et al.*,[14] are also given. It can be observed that our model gives results closer to those derived from HSPICE simulations than the previously published methods. The average error of the presented model is about 4.5%. In Fig. 9, the model is tested for two different sub-100 nm technologies (65 nm, 45 nm), transistor widths, output loads and supply voltages. Comparisons with BSIM4 HSPICE simulations indicate that the presented overshoot time period model (Eqs. (15)−(16)) is valid for a range of nanometer technologies, supply voltages, transistor widths and output loads. In addition, to test the developed model for narrow transistor widths, in Fig. 10, the overshoot time period during a rising input voltage transition is plotted as a function of the input voltage transition time. A supply voltage of 1.8 V and a load of 5 fF were used. The channel length of the used transistors was 90 nm, while the channel width was 100 nm and 250 nm for the NMOS and PMOS transistor, respectively. The comparison of the calculated results with those produced by BSIM4 HSPICE simulations, shows that the proposed model preserves its accuracy for narrow transistor widths.

Finally, in Fig. 11, the maximum output voltage obtained from the presented model (Eqs. (19)−(20)) is plotted as a function of input voltage transition time for



(a)



(b)

Fig. 8. Overshoot time period obtained from the presented model as a function of input voltage transition time for (a) slow and (b) fast input transitions and comparison with BSIM4 HSPICE simulations and models of previously published works.

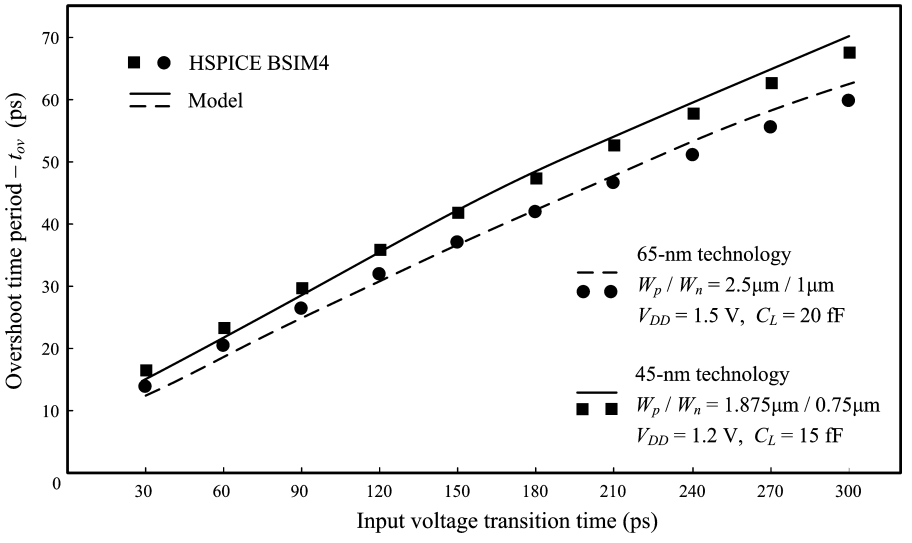


Fig. 9. Overshoot time period obtained from the presented model as a function of input voltage transition time and comparison with BSIM4 HSPICE simulations for two different sub-100 nm technologies, transistor widths, output loads and supply voltages.

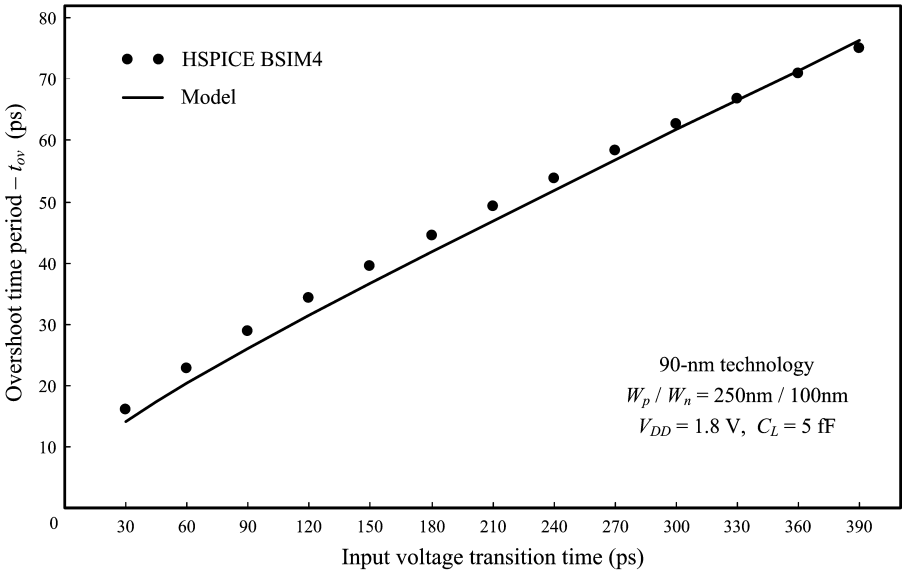


Fig. 10. Overshoot time period obtained from the presented model as a function of input voltage transition time and comparison with BSIM4 HSPICE simulations for narrow transistor widths.

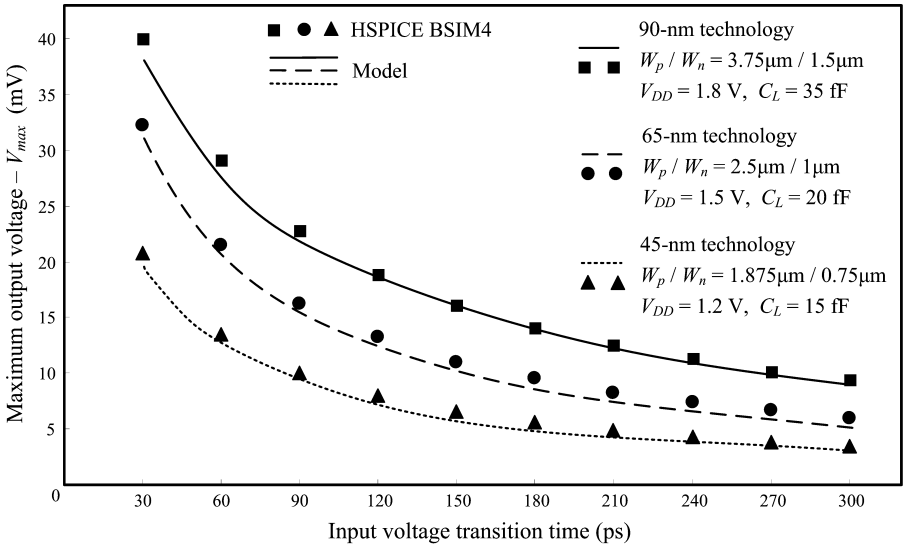


Fig. 11. Maximum output voltage obtained from the presented model as a function of input voltage transition time and comparison with BSIM4 HSPICE simulations for three different sub-100 nm technologies, transistor widths, output loads and supply voltages.

three different sub-100 nm technologies, transistor widths, output loads and supply voltages. Comparisons with BSIM4 HSPICE simulations show that the derived formula for the maximum output voltage gives accurate results. The model for both maximum output voltage and overshoot time period is analytical (i.e., derives closed-form expressions), does not use numerical procedures and is at least two orders of magnitude faster than HSPICE.

The presented model can also be applied to complex CMOS gates, since several fast methods[9,16,17] have been proposed for reducing a gate to an equivalent inverter. In addition, the proposed analytical model that uses purely capacitive load can be interfaced with methodologies, considering the effect of interconnects' resistance and inductance by using the effective capacitance of a distributed RC and/or RLC load.[28,29]

6. Conclusion

An analytical model for the overshooting effect of CMOS inverters in nanometer technologies has been presented. Analytical, accurate and fast computation of the overshoot time period and the maximum output voltage has been achieved. The model accounts for the influences of input voltage transition time, both transistors drain currents and sizes, gate-to-drain and load capacitances, and sub-100 nm device carrier velocity saturation and narrow-width effects. The results produced by the

model show very good agreement with BSIM4 HSPICE simulations and greater accuracy than those of previously published works.

Appendix A. Analytical Calculation of S and x'_{ov}

The current slope S is computed by equating the PMOS current in the linear region (Eq. (9)) with the approximated one (Eq. (13)), at the normalized time point: $x_c = (n + x'_{ov})/2$ (Fig. 6). x'_{ov} is the normalized time value at which the output voltage overshoot finishes with the assumption of negligible short-circuit (PMOS) current. The solution of the differential equation (11) for negligible PMOS current is:

$$u_{\text{out}} = u_n + (x - n)c_m - \frac{A_{sn}(x - n)^{a_n+1}}{a_n + 1}. \tag{A.1}$$

By equating u_{out} (as given by Eq. (14)) with 1, x'_{ov} is computed (to avoid numerical procedures the approximation $\alpha_n = 1$ is used):

$$x'_{ov} = n + \frac{c_m + \sqrt{2A_{sn}(u_n - 1) + c_m^2}}{A_{sn}}. \tag{A.2}$$

Note that, as indicated in Fig. 7, x'_{ov} is generally larger than x_{ov}, due to the fact that the PMOS drain current tends to lead the output node of the inverter to V_{DD}, and in the case of x'_{ov}, the PMOS drain current is neglected.

By equating the PMOS current in the linear region with the approximated one (Eq. (9) and Eq. (13), respectively), at the normalized time point x_c, the current slope S is obtained:

$$S = \frac{\begin{array}{c} 2dGk_{lp2}(H - F + 1) - dGM - 2 \\ +\sqrt{(dGM + 2)^2 - 4dGk_{lp2}(2H - 2F + dGI_{p(n)} + 2)} \end{array}}{d^2G^3k_{lp2}}, \tag{A.3}$$

where $F = u_n + c_mG + I_{p(n)}dG$, $G = x_c - n$, $H = \frac{A_{sn}G^{a_n+1}}{a_n+1}$, and $M = k_{lp1}(1 - x_c - p)^{a_p/2}$.

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